

Total Pages	Page
28	1

Product Standards

Part No.	NN30295A
Package Code No.	HQFN024-A3-0404A

	Product Standards	NN30295A	
		Total Pages	Page
		28	2

Contents

■ Overview	3
■ Features	3
■ Applications	3
■ Package	3
■ Type	3
■ Application Circuit Example (Block Diagram)	4
■ Pin Descriptions	5
■ Absolute Maximum Ratings	6
■ Operating Supply Voltage Range	6
■ Allowable Current and Voltage Range	7
■ Electrical Characteristics	8
■ Electrical Characteristics (Reference values for design)	9
■ Test Circuit Diagram	13
■ Technical Data	14
1. I/O block circuit diagrams and pin function descriptions	14
2. Power ON / OFF sequence	18
3. Protection	19
4. Output Voltage Setting	20
5. Soft Start Setting	20
6. I ² C-bus Interface	21
7. Register Map	23
■ Usage Notes	22
• Attention and precaution in using	26
• Special attention and precaution in using	28

	Product Standards	NN30295A	
		Total Pages	Page
		28	3

NN30295A

6A Synchronous DC DC Step down Regulator

comprising of Controller IC and Power MOSFET with I²C Interface.

■ Overview

NN30295A is a synchronous DCDC Step Down regulator (1-ch) comprising of a Controller IC and two Power MOSFETs, and employs a hysteretic control system. This system responds rapidly to sudden variations in load current, thus maintaining the fluctuations in the output voltage to a minimum level. The system does not require external components for phase compensation. Together with the use of capacitors with small capacitance, this IC realizes downsizing of the set and reduces to a great extent, the number of external parts required for the system.

Output voltage is adjustable by the User. Maximum current is 6A.

■ Features

- High-speed response step-down DCDC regulator circuit that employs hysteretic control system
- Integrated Two 25m Ω (Typ) MOSFET for high efficiency at 6A
- Mode Selection Option via I²C:
 - (1) Pulse Skip Mode (PSM) with coast mode function for high light load efficiency
 - (2) Forced Continuous Conduction Mode (FCCM) for quick load transient response
- Input Voltage Range: AV_{IN}: 4.5V to 5.6V , PV_{IN}: 3.1V to 5.6V , VDD: 1.7V to 3.3V
- Output Voltage Range: 0.6V to 3.5V
- Selectable Switching Frequency 500kHz to 2MHz (7 steps) using I²C; Default = 1MHz
- Adjustable Soft Start (SS) Via External Capacitor
- Low Operating and Standby Quiescent Current
- Open Drain Power Good (PGOOD) Indication for Output Over/Under-Voltage
- Built-in Under Voltage Lockout (UVLO), Thermal Shut Down (TSD), Output Over-voltage Detection (OVD), Under Voltage Detection (UVD), Output Over-Current Protection (OCP) and Short Circuit Protection (SCP) function
- Fast mode I²C interface to control the output voltage level

■ Applications

- High Current Distributed Power Systems such as Hard Disk Drives (HDD), Solid State Drives (SSD), Portable phones, Security Cameras, Network TVs, Home Appliances, OA Equipment, Notebook PCs, Server & Desktop computers etc.

■ Package

- 24pin Plastic Quad Flat Non-leaded Package Heat Slug Down (QFN Type)
(Size : 4 mm \times 4 mm, 0.5 mm pitch)

■ Type

- Multichip IC

Product Standards

NN30295A

Total Pages

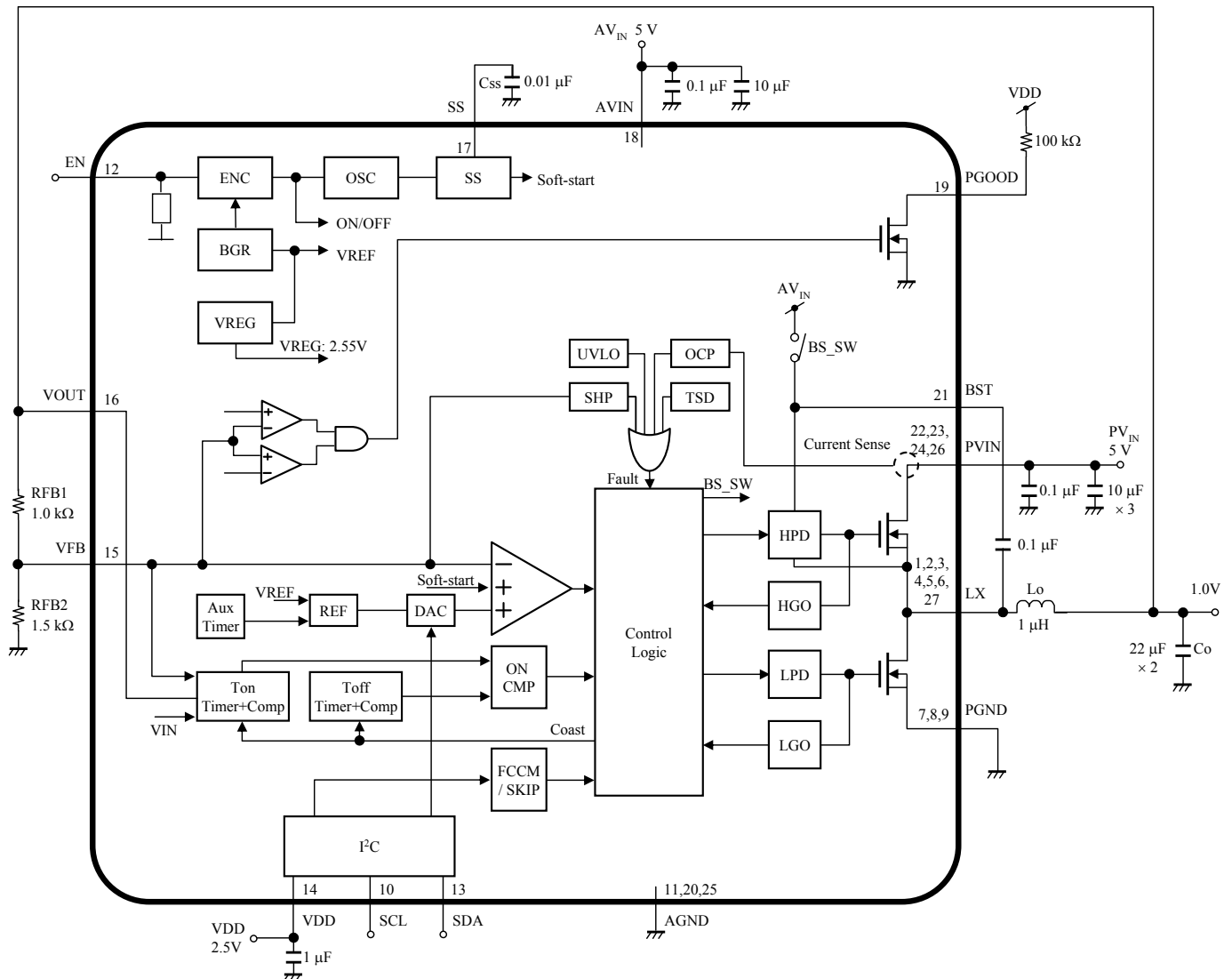
Page

28

4

Application Circuit Example (Block Diagram)

Typical Condition: $AV_{IN} = PV_{IN} = 5V$, $VDD = 2.5V$, $V_{OUT} = 1.0V$, $I_{OUT} = 6A$, $F_{sw} = 1MHz$

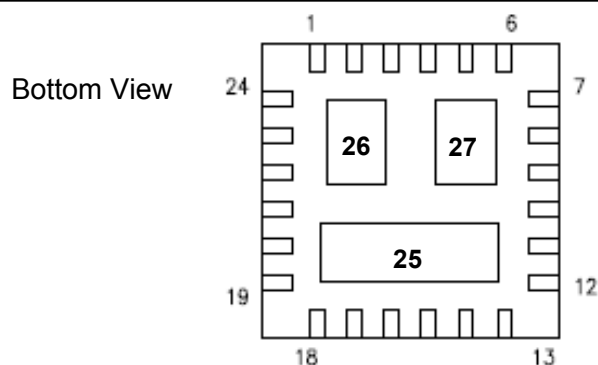


- Notes)
- This application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The User is fully responsible for the incorporation of the above illustrated application circuit and the information attached with it, in the design of the equipment.
 - This block diagram explains the major functions of the IC. Part of the block diagram may be omitted, or simplified.

	<h1>Product Standards</h1>	NN30295A	
		Total Pages	Page
		28	5

■ Pin Descriptions

Pin No.	Pin name	Type	Description
1	LX	Output	Power MOSFET output pin
2	LX	Output	Power MOSFET output pin
3	LX	Output	Power MOSFET output pin
4	LX	Output	Power MOSFET output pin
5	LX	Output	Power MOSFET output pin
6	LX	Output	Power MOSFET output pin
7	PGND	Ground	Ground pin for Power MOSFET
8	PGND	Ground	Ground pin for Power MOSFET
9	PGND	Ground	Ground pin for Power MOSFET
10	SCL	Input	I ² C Interface Clock Input pin
11	AGND	Ground	Analog Ground pin
12	EN	Input	ON/OFF control pin
13	SDA	Input/Output	I ² C Interface Data I/O pin
14	VDD	Power Supply	Power supply pin for Digital Circuit
15	VFB	Input	Feed Back pin
16	VOUT	Input	Output voltage sense pin
17	SS	Input	Soft-Start pin, Connect external capacitor
18	AVIN	Power Supply	Controller Power supply pin
19	PGOOD	Output	Power good flap pin (open drain)
20	AGND	Ground	Analog Ground pin
21	BST	Input	Supply input pin for high side FET gate driver (boost terminal)
22	PVIN	Power supply	Power supply pin for Power MOSFET
23	PVIN	Power supply	Power supply pin for Power MOSFET
24	PVIN	Power supply	Power supply pin for Power MOSFET
25	AGND	Ground	Ground pin for radiation of heat
26	PVIN	Power supply	Power supply pin
27	LX	Output	Power MOSFET output pin



	Product Standards	NN30295A	
		Total Pages	Page
		28	6

■ Absolute Maximum Ratings

Note) Absolute maximum ratings are limit values which do not result in damages to this IC, and IC operation is not guaranteed at these limit values.

A No.	Parameter	Symbol	Rating	Unit	Notes
1	Supply voltage	V_{IN}	6.0	V	*1
		VDD	3.6	V	*1
2	Supply current	I_{IN}	—	A	—
3	Power dissipation	P_D	178	mW	*2
4	Operating ambient temperature	T_{opr}	−40 to +85	°C	*3
5	Storage temperature	T_{stg}	−55 to +150	°C	*3

Notes) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

V_{IN} is voltage for AVIN, PVIN. VDD is voltage for VDD.

*2 : The power dissipation shown is the value at $T_a = 85^\circ\text{C}$ for the independent (unmounted) IC package without a heat sink.
When using this IC, refer to the P_D - T_a Power Dissipation Curve provided under the Technical Report in the Usage Notes.
Sufficient margin must be used in the Heat Radiation design so that the Power dissipation value is not exceeded,
based on the conditions of power supply voltage, load, and ambient temperature.

*3 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for $T_a = 25^\circ\text{C}$.

■ Operating Supply Voltage Range

Parameter	Symbol	Range	Unit	Notes
Supply voltage range - Controller	AV_{IN}	4.5 to 5.6	V	*1
Supply voltage range - Power	PV_{IN}	3.1 to 5.6	V	*1
Supply voltage range - I^2C	VDD	1.7 to 3.3	V	*1

Note) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

AV_{IN} is the voltage for AVIN; PV_{IN} is the voltage for PVIN; VDD is the voltage for VDD.

	Product Standards	NN30295A	
		Total Pages	Page
		28	7

■ Allowable Current and Voltage Range

- Notes)
- Allowable current and voltage ranges are limit ranges which do not result in damages to this IC.
IC operation is not guaranteed within these limit ranges.
 - Voltage values, unless otherwise specified, are with respect to GND.
GND is the voltage for AGND, PGND. GND = AGND = PGND.
 - V_{IN} is the voltage for AV_{IN} , PV_{IN} . $AV_{IN} = PV_{IN}$.
 - Do not apply external currents or voltages to any pin not specifically mentioned.

Pin No.	Pin name	Rating	Unit	Notes
1,2,3, 4,5,6, 27	LX	-0.3 to $(V_{IN} + 0.3)$	V	*1
12	EN	-0.3 to $(V_{IN} + 0.3)$	V	*1
13	SDA	-0.3 to $(VDD + 0.3)$	V	*1
10	SCL	-0.3 to $(VDD + 0.3)$	V	*1
19	PGOOD	-0.3 to $(V_{IN} + 0.3)$	V	*1

Note) *1 : $(V_{IN} + 0.3)$ V must not exceed 6 V , $(VDD + 0.3)$ V must not exceed 3.6 V

	Product Standards	NN30295A	
		Total Pages	Page
		28	8

■ Electrical Characteristics at $V_{IN} = AV_{IN} = PV_{IN} = 5\text{ V}$, $VDD = 2.5\text{ V}$

Note1) $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$ unless otherwise specified.

Note2) Switching Frequency = 1 MHz unless otherwise specified.

B No.	Parameter	Symbol	Test circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
[DCDC] (DCDC Step-down Regulator) Condition : C _o = 22 μF × 2 (Murata), L _o = 1 μH (Panasonic), V _{OUT} Setting = 1.0V, Mode = Pulse Skip Mode (PSM), unless otherwise specified.									
[Current Consumption]									
1	Consumption current : Active	IVDDACT	1	EN = 5 V RFB1 = 1.0 kΩ RFB2 = 1.5 kΩ I _{OUT} = 0 A	—	400	700	μA	—
2	Consumption current : Standby	IVDDSTB	1	EN = 0 V I _{OUT} = 0 A	—	—	2	μA	—
[Enable Pin Characteristics]									
3	EN pin Low level input voltage	VEN1L	1	V _{IN} = 5 V	−0.3	—	0.3	V	—
4	EN pin High level input voltage	VEN1H	1	V _{IN} = 5 V	1.5	—	V _{IN} +0.3	V	—
5	EN pin leak current	ILEAKEN1	1	EN = 5 V	—	3.5	10	μA	—
[Internal Reference Characteristics]									
6	VFB comparator threshold	VFBTS	1	—	0.595	0.603	0.611	V	—
[Under Voltage Lock Out]									
7	PVIN UVLO trigger voltage	VUVLODET1	1	PV _{IN} = 5 V → 0 V	2.45	2.60	2.75	V	—
8	PVIN UVLO hysteresis voltage	VUVLOHYS1	1	PV _{IN} = 0 V → 5 V	50	200	350	mV	—
9	AVIN UVLO trigger voltage	VUVLODET2	1	AV _{IN} = 5 V → 0 V	3.25	3.40	3.55	V	—
10	AVIN UVLO hysteresis voltage	VUVLOHYS2	1	AV _{IN} = 0 V → 5 V	10	100	250	mV	—
11	VDD UVLO trigger voltage	VUVLODET3	1	VDD = 3 V → 0 V	1.00	1.25	1.50	V	—
12	VDD UVLO hysteresis voltage	VUVLOHYS3	1	VDD = 0 V → 3 V	10	50	90	mV	—
[PGOOD Pin Characteristics]									
13	PGOOD Threshold 1 (VFB ratio for UVD detect)	VTHPG1	1	PGOOD = L → H	78	85	92	%	—
14	PGOOD Hysteresis 1 (UVD hysteresis)	VHYSPG1	1	PGOOD = H → L	2	5	8	%	—
15	PGOOD Threshold 2 (VFB ratio for OVD detect)	VTHPG2	1	PGOOD = L → H	108	115	122	%	—
16	PGOOD Hysteresis 2 (OVD hysteresis)	VHYSPG2	1	PGOOD = H → L	2	5	8	%	—
17	PGOOD ON resistance	RPG	1	EN = 0 V	—	10	15	Ω	—

	Product Standards	NN30295A	
		Total Pages	Page
		28	9

■ Electrical Characteristics (Reference values for design) at $V_{IN} = AV_{IN} = PV_{IN} = 5\text{ V}$, $VDD = 2.5\text{ V}$

Note1) $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$ unless otherwise specified.

Note2) Switching Frequency = 1 MHz unless otherwise specified.

The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.

If a problem does occur related to these characteristics, we will respond in good faith to the user's concerns.

B No.	Parameter	Symbol	Test circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
[DCDC] (DCDC Step-down Regulator) Condition : C _o = 22 μF × 2 (Murata), L _o = 1 μH (Panasonic), V _{OUT} Setting = 1.0V, Mode = Pulse Skip Mode (PSM), unless otherwise specified.									
[I ² C Bus (Internal I/O Stage Characteristics)]									
18	Low-level input voltage	VIL1	1	Voltage which recognized that SDA and SCL are Low-level	−0.5	—	0.3× VDD	V	*1
19	High-level input voltage	VIH1	1	Voltage which recognized that SDA and SCL are High-level	0.7× VDD	—	VDD _{max} +0.5	V	*1
20	Low-level output voltage 1	VOL1	1	VDD > 2V SDA (sink current=3mA)	0	—	0.4	V	—
21	Low-level output voltage 2	VOL2	1	VDD < 2V SDA (sink current=3mA)	0	—	0.2× VDD	V	—
22	Input current each I/O pin	IL	1	SDA, SCL = 0.1 × VDD _{max} to 0.9 × VDD _{max}	−10	—	10	μA	—
23	SCL clock frequency	FOSC	1	—	0	—	400	kHz	—

Note) *1 : The input threshold voltage of I²C bus (Vth) is linked to VDD.

In case the pull-up voltage is not VDD, the threshold voltage (Vth) is fixed to $((VDD / 2) \pm (\text{Schmitt width} / 2))$ and High-level, Low-level of input voltage are not specified.

In this case, pay attention to Low-level (max.) value (V_{ILmax}).

It is recommended that the pull-up voltage of I²C bus is set to the I²C bus I/O stage supply voltage (VDD).

	Product Standards	NN30295A	
		Total Pages	Page
		28	10

■ Electrical Characteristics (Reference values for design) at $V_{IN} = AV_{IN} = PV_{IN} = 5\text{ V}$, $V_{DD} = 2.5\text{ V}$

Note1) $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$ unless otherwise specified.

Note2) Switching Frequency = 1 MHz unless otherwise specified.

The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.

If a problem does occur related to these characteristics, we will respond in good faith to the user's concerns.

B No.	Parameter	Symbol	Test circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
[DCDC] (DCDC Step-down Regulator) Condition : C _o = 22 μF × 2 (Murata), L _o = 1 μH (Panasonic), V _{OUT} Setting = 1.0V, Mode = Pulse Skip Mode (PSM), unless otherwise specified.									
[DCDC Characteristics]									
24	DCDC line regulation	DDREGIN	1	V _{IN} = 4.5 V → 5.6 V I _{OUT} = −4 A	—	0.5	1.5	%/V	—
25	DCDC load regulation	DDREGLD	1	I _{OUT} = −10 mA → −6 A	—	3	6	%	—
26	DCDC output current limit	DDILMT	1	—	6.1	9	13	A	—
27	DCDC efficiency 1 : Light Load	DDEFF1	1	V _{OUT} = 1.0 V I _{OUT} = −10 mA	60	70	—	%	—
28	DCDC efficiency 2 : Heavy Load	DDEFF2	1	V _{OUT} = 1.0 V I _{OUT} = −4 A	71	81	—	%	—
29	DCDC output ripple voltage 1	DDVRPL1	1	I _{OUT} = −10 mA	—	25	40	mV [p-p]	—
30	DCDC output ripple voltage 2	DDVRPL2	1	I _{OUT} = −4 A	—	10	20	mV [p-p]	—
31	DCDC load transient response	DDDVAC	1	I _{OUT} = −100 mA ↔ −4 A Δt = 0.5 A / μs	—	—	35	mV	—
32	DCDC High Side MOS ON resistance	DDRONH	1	V _{GS} = 5 V	—	25	50	mΩ	—
33	DCDC Low Side MOS ON resistance	DDRONL	1	V _{GS} = 5 V	—	25	50	mΩ	—
[Protection]									
34	DCDC Output GND Short Protection Threshold	DDSHPTH	1	FB = 0.6 V → 0 V	55	70	85	%	—

	Product Standards	NN30295A	
		Total Pages	Page
		28	11

■ Electrical Characteristics (Reference values for design) at $V_{IN} = AV_{IN} = PV_{IN} = 5\text{ V}$, $V_{DD} = 2.5\text{ V}$

Note1) $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$ unless otherwise specified.

Note2) Switching Frequency = 1 MHz unless otherwise specified.

The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.

If a problem does occur related to these characteristics, we will respond in good faith to the user's concerns.

B No.	Parameter	Symbol	Test circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
[DCDC] (DCDC Step-down Regulator) Condition : C _o = 22 μF × 2 (Murata), L _o = 1 μH (Panasonic), V _{OUT} Setting = 1.0V, Mode = Pulse Skip Mode (PSM), unless otherwise specified.									
[Soft-Start Timing]									
35	SS Charge Current	ISSCHG	1	V _{SS} = 0.3 V	−4	−2	—	μA	—
36	SS Discharge Resistance	RSSDIS	1	EN = 0 V I _{OUT} = 0 A	—	2	4	kΩ	—
[Switching Frequency Adjustment]									
37	DCDC Switching Frequency 1	DDFSW1	1	I _{OUT} = −6 A , I ² C Setting: 10h:10h	375	500	625	kHz	—
38	DCDC Switching Frequency 2	DDFSW2	1	I _{OUT} = −6 A , I ² C Setting: 10h:30h	750	1000	1250	kHz	—
39	DCDC Switching Frequency 3	DDFSW3	1	I _{OUT} = −6 A , I ² C Setting: 10h:70h	1500	2000	2500	kHz	—
[VFB Characteristics]									
40	VFB pin leak current 1	ILEAKFB1	1	VFB = 0 V	−1	—	1	μA	—
41	VFB pin leak current 2	ILEAKFB2	1	VFB = 3.6 V	−1	—	1	μA	—
[DCDC]									
42	Minimum Input and output voltage difference	DV	1	DV = PVIN − Vout > 2 V	2	—	—	V	—
[I ² C bus (Internal I/O stage characteristics)]									
43	Hysteresis of Schmitt trigger input 1	V _{hys1}	1	V _{IO} > 2 V, Hysteresis 1 of SDA, SCL	0.05× VDD	—	—	V	*1
44	Hysteresis of Schmitt trigger input 2	V _{hys2}	1	V _{IO} < 2 V, Hysteresis 2 of SDA, SCL	0.1× VDD	—	—	V	*1
45	Output fall time from V _{IHmin} to V _{ILmax}	T _{of}	1	Bus capacitance : 10pF to 400pF I _P ≤ 6 mA, (V _{OLmax} = 0.6 V) I _P : Max. sink current	20+ 0.1×C _b	—	250	ns	*1
46	Pulse width of spikes which must be suppressed by the input filter	T _{sp}	1	—	0	—	50	ns	*1
47	Capacitance for each I/O pin	C _i	1	—	—	—	10	pF	*1

Note) *1 : The timing of Fast-mode devices in I²C-bus is specified as the following.

All values referred to V_{IHmin} and V_{ILmax} level.

	Product Standards	NN30295A	
		Total Pages	Page
		28	12

■ Electrical Characteristics (Reference values for design) at $V_{IN} = AV_{IN} = PV_{IN} = 5\text{ V}$, $V_{DD} = 2.5\text{ V}$

Note1) $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$ unless otherwise specified.

Note2) Switching Frequency = 1 MHz unless otherwise specified.

The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.

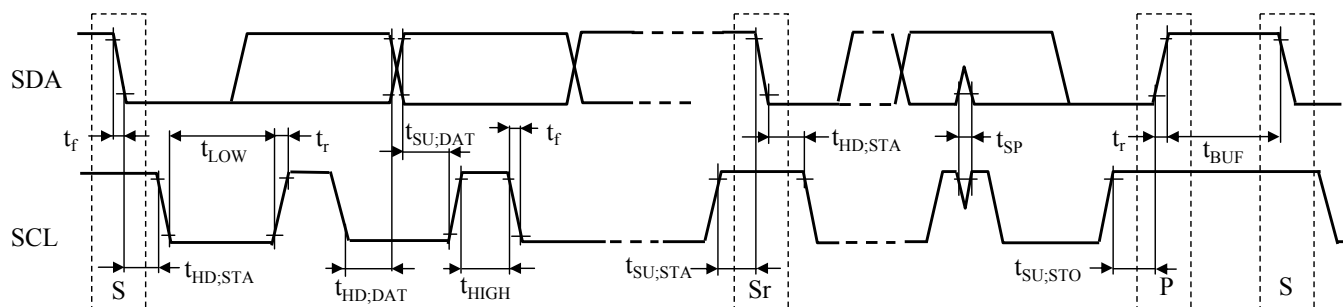
If a problem does occur related to these characteristics, we will respond in good faith to the user's concerns.

B No.	Parameter	Symbol	Test circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
[I ² C bus (Bus line specifications)]									
48	Hold time (repeated) START condition	t _{HD:STA}	1	The first clock pulse is generated after t _{HD:STA} .	0.6	—	—	μs	*1
49	Low period of the SCL clock	t _{LOW}	1	—	1.3	—	—	μs	*1
50	High period of the SCL clock	t _{HIGH}	1	—	0.6	—	—	μs	*1
51	Set-up time for a repeat START condition	t _{SU:STA}	1	—	0.6	—	—	μs	*1
52	Data hold time	t _{HD:DAT}	1	—	0	—	0.9	μs	*1
53	Data set-up time	t _{SU:DAT}	1	—	100	—	—	ns	*1
54	Rise time of both SDA and SCL signals	t _r	1	—	20+ 0.1×C _b	—	300	ns	*1 *2
55	Fall time of both SDA and SCL signals	t _f	1	—	20+ 0.1×C _b	—	300	ns	*1 *2
56	Set-up time of STOP condition	t _{SU:STO}	1	—	0.6	—	—	μs	*1
57	Bus free time between STOP and START condition	t _{BUF}	1	—	1.3	—	—	μs	*1
58	Capacitive load for each bus line	C _b	1	—	—	—	400	pF	*1
59	Noise margin at the Low-level for each connected device	V _{nL}	1	—	0.1× VDD	—	—	V	*1
60	Noise margin at the High-level for each connected device	V _{nH}	1	—	0.2× VDD	—	—	V	*1

Note) *1 : The timing of Fast-mode devices in I²C-bus is specified as the following.

All values referred to V_{IHmin} and V_{ILmax} level.

*2 : For Standard-mode I²C devices, the minimum limits for t_r and t_f are not specified.



S : START condition

Sr : Repeat START condition

P : STOP condition

Product Standards

NN30295A

Total Pages

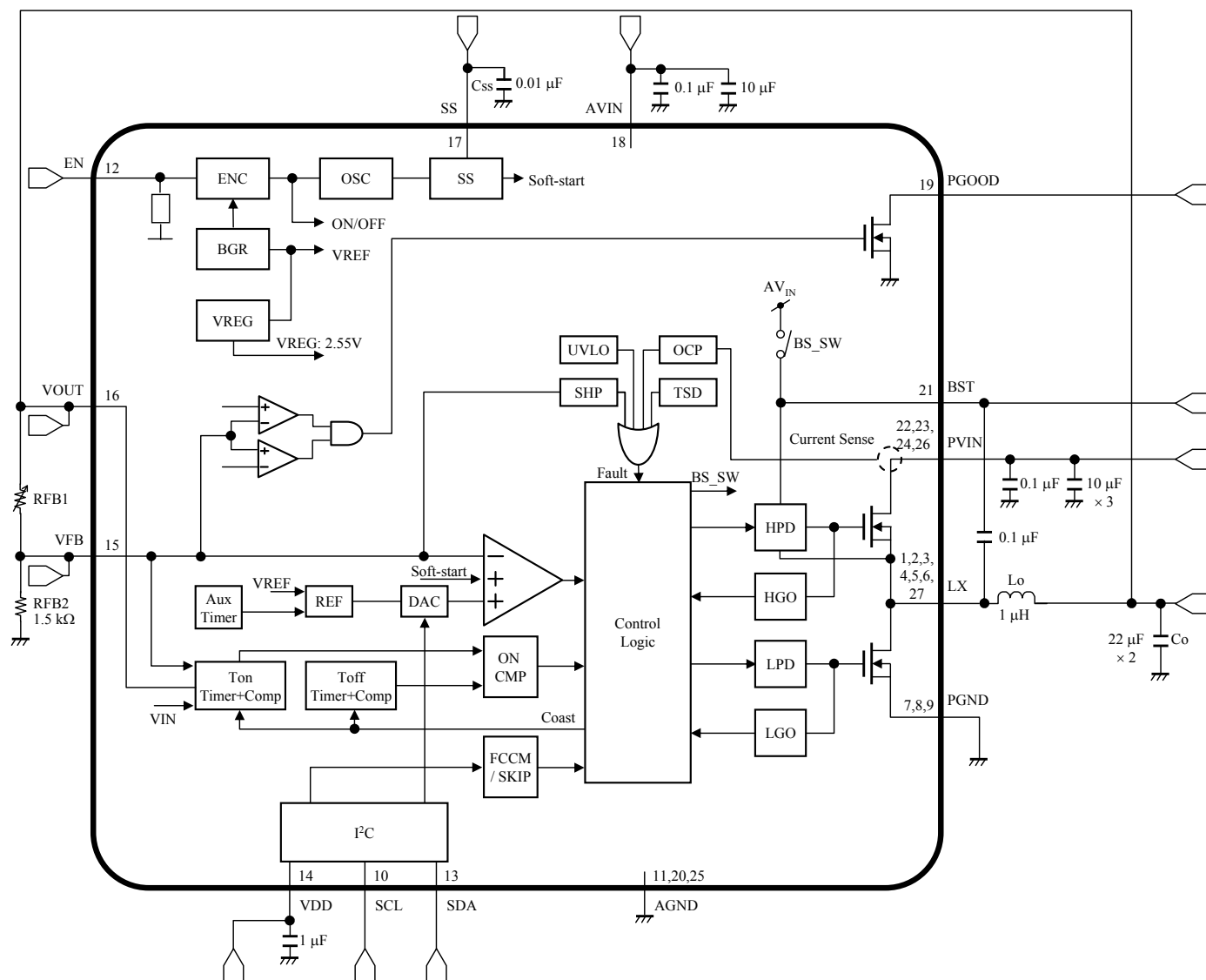
Page

28

13

Test Circuit Diagram

1. Test Circuit 1



	<h1>Product Standards</h1>	NN30295A	
		Total Pages	Page
		28	14

■ Technical Data

1. I/O block circuit diagrams and pin function descriptions

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

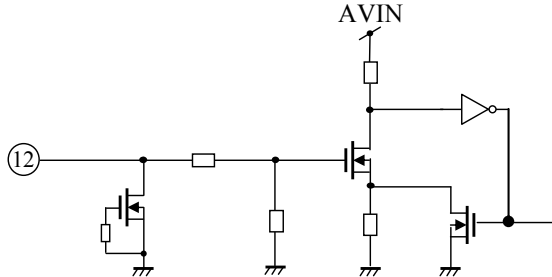
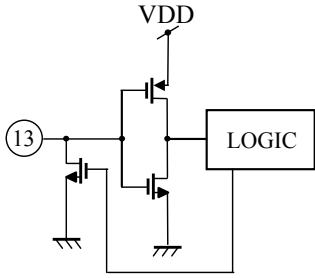
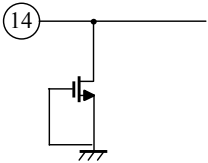
Pin No.	Pin Name	Waveform and voltage	Internal circuit	Impedance	Description
1	LX	0 V to V_{IN}		—	Power MOSFET output pin
2					
3					
4					
5					
6					
27					
21	BST	AV_{IN} to $2 \times AV_{IN}$		—	Supply input for high side FET gate driver pin
7	PGND	0 V		—	Ground pin for Power MOSFET
8					
9					
10	SCL	0 V to VDD		—	I ² C Interface for Clock Input pin
11	AGND	0 V		—	Ground pin
20					
25					

	Product Standards	NN30295A	
		Total Pages	Page
		28	15

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

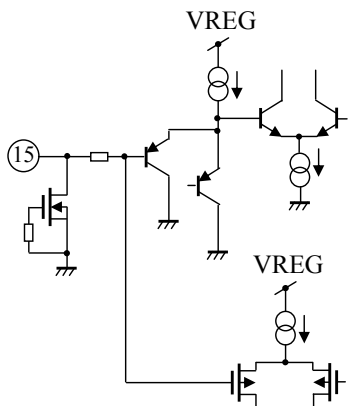
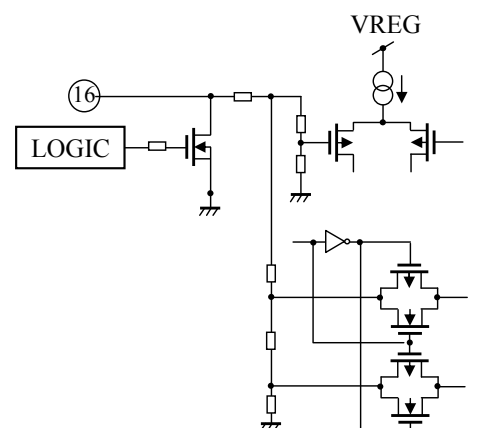
Pin No.	Pin Name	Waveform and voltage	Internal circuit	Impedance	Description
12	EN	0 V to V_{IN}		2000 k Ω	ON/OFF control pin
13	SDA	0 V to VDD		—	I ² C Interface for Data I/O pin
14	VDD	VDD		—	Power supply Pin For Digital Circuit

	Product Standards	NN30295A	
		Total Pages	Page
		28	16

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Pin Name	Waveform and voltage	Internal circuit	Impedance	Description
15	VFB	about 0.6 V		—	Comparator negative input pin
16	VOUT	0.6V to 3.5 V		225 kΩ	Output voltage sense pin

Product Standards

NN30295A

Total Pages

Page

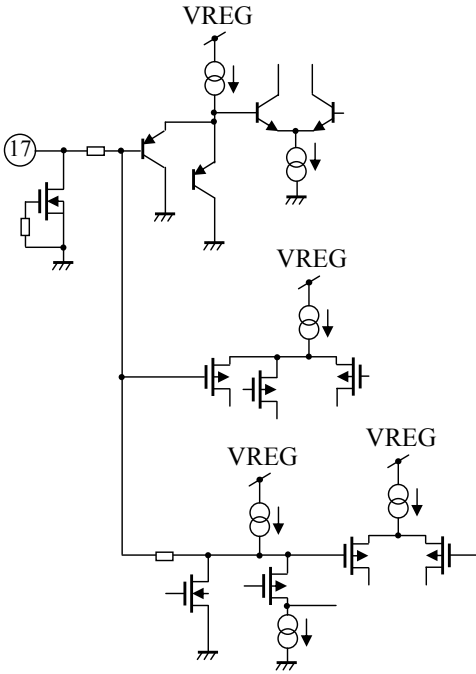
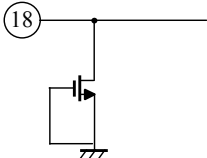
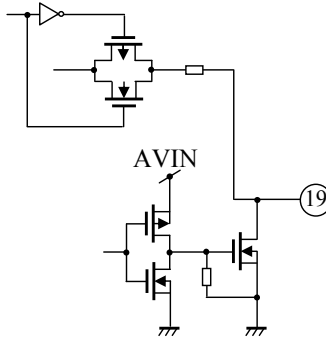
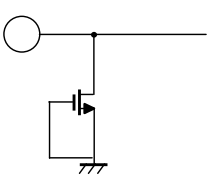
28

17

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

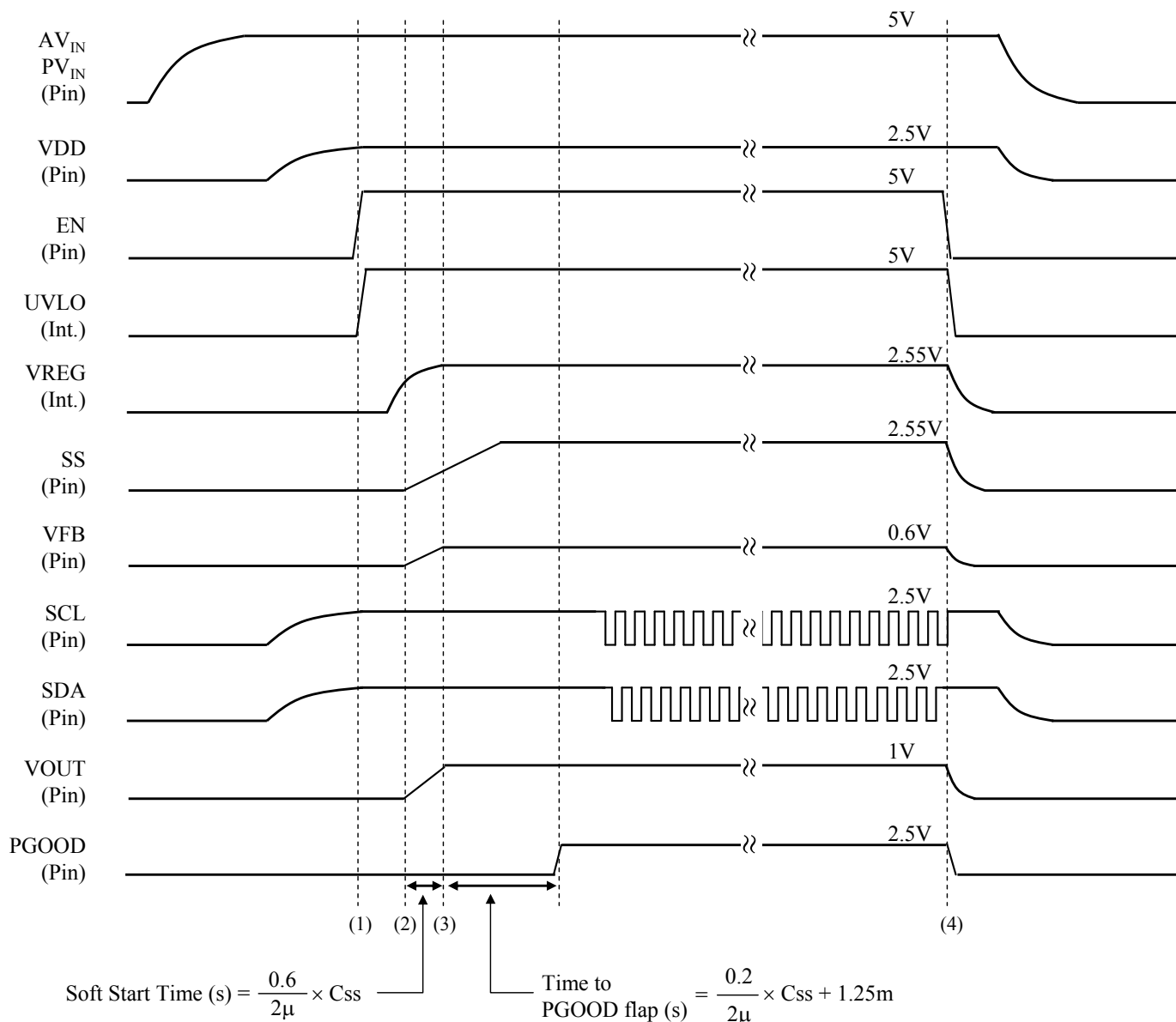
Pin No.	Pin Name	Waveform and voltage	Internal circuit	Impedance	Description
17	SS	0V to VREG		—	Soft start capacitor connect pin
18	AVIN	V_{IN}		—	Power supply pin for controller
19	PGOOD	0V to V_{IN}		—	Power good open drain pin
22	PVIN	V_{IN}	<p>Pin 22, 23 24, 26</p> 	—	Power supply pin for Power MOSFET
23					
24					
26					

	Product Standards	NN30295A	
		Total Pages	Page
		28	18

■ Technical Data (continued)

2. Power ON / OFF sequence

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.



- (1) When the EN pin is set to "High" after the V_{IN} settles, the UVLO is released after VIN exceeds its threshold.
- (2) The UVLO is released followed by the VREG start-up. The SOFT START sequence is when the VREG exceeds its threshold and the capacitor connected to the SS pin begins to charge. The SS pin voltage increases linearly.
- (3) The VOUT pin (DCDC Output) voltage increases at the same rate as the SS pin.
Normal operation begins after the VOUT pin reaches the set voltage.
- (4) When the EN pin is set to "Low", the VREG and UVLO stop operation and the VOUT pin / SS pin voltage drops to 0V.

Note: (1) The SS pin capacitor should be discharged completely before restarting the startup sequence.
An incomplete discharge process might result in an overshoot of the output voltage.

	Product Standards	NN30295A	
		Total Pages	Page
		28	19

■ Technical Data (continued)

3. Protection

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

- Output Over-Current Protection (OCP) function and Short-Circuit Protection (SCP) function

- (1) The Over-Current Protection is activated at about 9A (Typ.)
During the OCP, the output voltage continues to drop at the specified current.
- (2) The Short-Circuit Protection function is implemented when the output voltage decreases and the VFB pin reaches to about 70% of the set voltage.
- (3) The SCP operates intermittently at 2ms-ON, 16ms-OFF intervals.

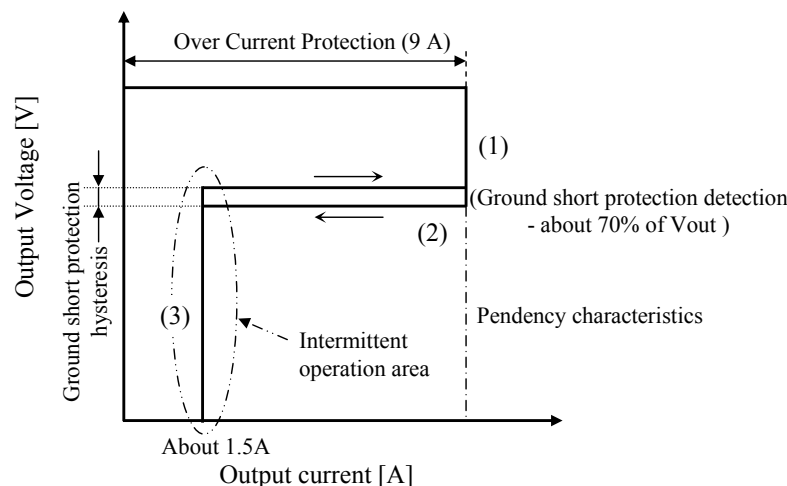


Figure : OCP and SCP Operation

- Over Voltage Detection (OVD) and Under Voltage Detection (UVD)

- (1) The NMOS connected to the PGOOD pin turns ON when the output voltage rises and the VFB pin voltage reaches 115% of its set voltage. The VOUT pin voltage is discharged by internal MOSFET until 110% of its set voltage.
- (2) After (1) above, the NMOS connected to the PGOOD pin is turned OFF turned OFF after 1 ms when the output voltage drops and the VFB pin voltage reaches 110% of its set voltage.
- (3) The NMOS connected to the PGOOD pin turns ON when the output voltage drops and the VFB pin voltage reaches 85% of its set voltage.
- (4) After (3) above, the NMOS connected to the PGOOD pin is turned OFF after 1 ms when the output voltage drops and the VFB pin voltage reaches 90% of its set voltage.

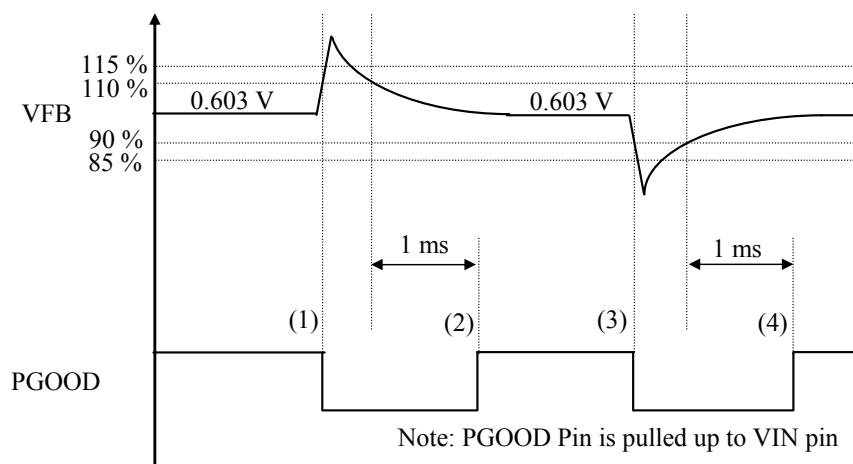


Figure : OVD and UVD Operation

- Thermal Shut Down (TSD)

When the IC internal temperature becomes more than about 140°C, TSD operates and DCDC turns off..

	Product Standards	NN30295A	
		Total Pages	Page
		28	20

■ Technical Data (continued)

4. Output Voltage Setting

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

• Output Voltage Settings

The output voltage is set by adjusting the value of the external resistors RFB1 and RFB2.

The equation below represents the relation between the external resistors and the VOUT.

(VIN = 5 V, IOUT = -1 A, PSM, Fsw = 1 MHz)

$$V_{OUT} = -0.0119 \left(\frac{R_{FB1}}{R_{FB2}} \right)^2 + 0.616 \left(\frac{R_{FB1}}{R_{FB2}} \right) + 0.593$$

The following table represents the Feedback Resistor (RFB) settings for common Output Voltages

Table : Recommended settings for Common Output Voltages

VOUT [V]	RFB1 [kΩ]	RFB2 [kΩ]
1.8	3.0	1.5
1.2	1.0	1.0
1.0	1.0	1.5

Note: RFB2 can be set to a maximum value of 10kΩ. A larger FBR2 value will be more susceptible to noise.

VFB comparator threshold is adjusted to ± 1.33%, but the actual output voltage accuracy becomes more than ± 1.33% due to the influence from the circuits other than VFB comparator.

In the case of VOUT=1.0V, the actual output voltage accuracy becomes ±2.0% (VIN=5V, IOUT= -1A, PSM, Fsw=1MHz).

5. Soft Start Setting

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

• Soft Start Setting

Soft Start function maintains the smooth control of the output voltage during start up by adjusting the soft start time.

When the EN pin becomes "High", a current of 2uA begins to charge the external capacitor (C_{SS}) at the SS pin, and the SS pin voltage increases linearly. The SS pin voltage controls the FB pin voltage resulting in a linear increase in the FB pin voltage. The FB voltage remains constant after its designed value is reached.

On the other hand, the SS pin voltage continues to increase up to the designed value of about 2.55V.

The calculation of Soft Start Time is as follows.

$$\text{Soft Start Time (sec)} = \frac{0.6}{2\mu} \times C_{SS}$$

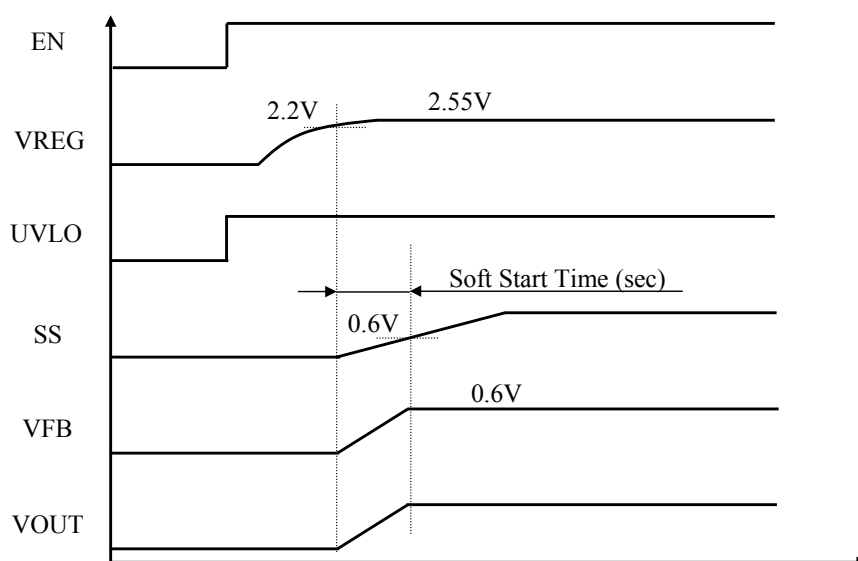


Figure : Soft Start Operation

	Product Standards	NN30295A	
		Total Pages	Page
		28	21

■ Technical Data (continued)

6. I²C-bus Interface

a.) Basic Rules

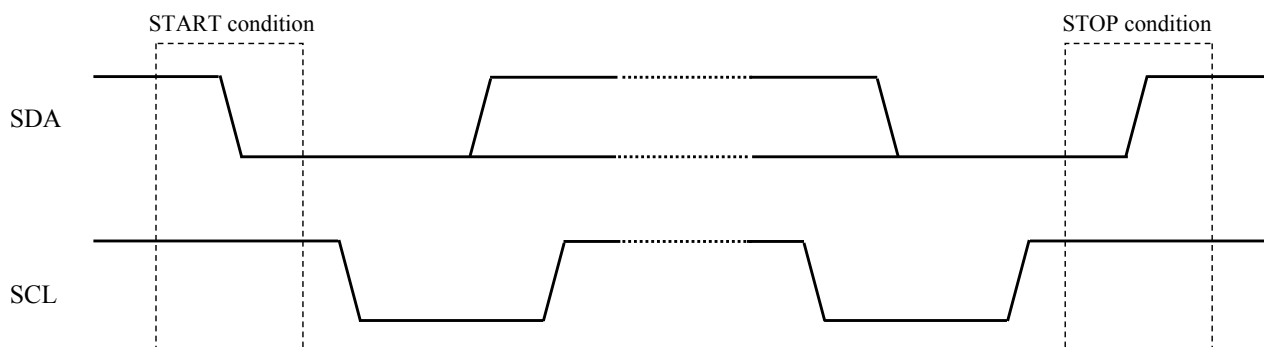
- This IC, I²C-bus, is designed to correspond to the Standard-mode (100 kbps) and Fast-mode(400 kbps) devices in the version 2.1 of NXP's specification. However, it does not correspond to the H_S-mode (to 3.4 Mbps).
- This IC will operate as a slave device in the I²C-bus system. This IC will not operate as a master device.
- The program operation check of this IC has not been conducted on the multi-master bus system and the mix-speed bus system, yet. The connected confirmation of this IC to the CBUS receiver also has not been checked. Please confirm with our company if the IC will be used in these mode systems.
- The I²C is the brand of NXP.

b.) START and STOP conditions

A High to Low transition on the SDA line while SCL is High is one such unique case. This situation indicates START condition. A Low to High transition on the SDA line while SCL is High defines STOP condition.

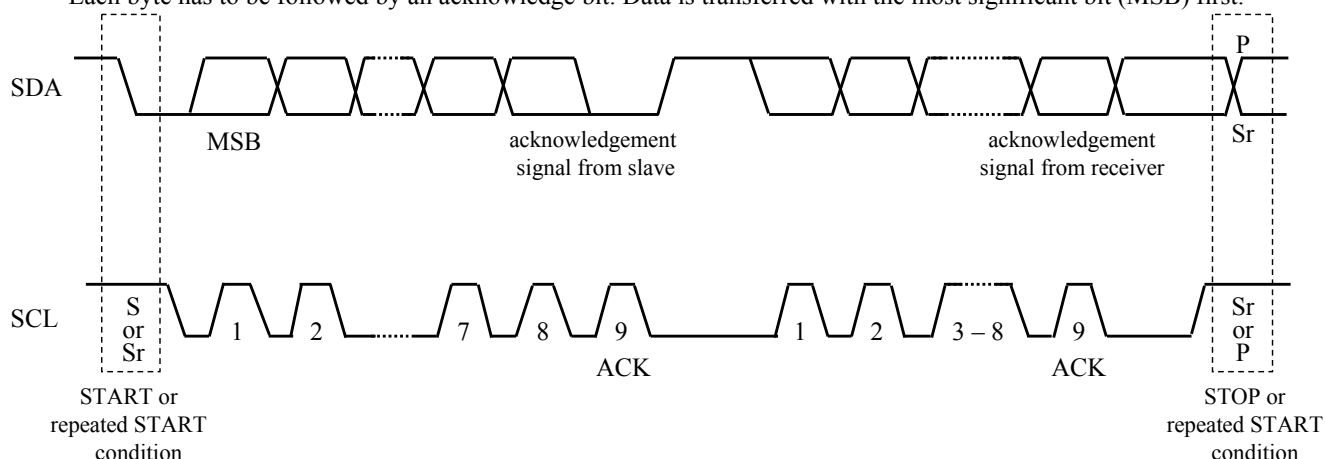
START and STOP conditions are always generated by the master. After START condition occur, the bus will be busy.

The bus is considered to be free again a certain time after the STOP condition.



c.) Transferring Data

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.



	Product Standards	NN30295A	
		Total Pages	Page
		28	22

■ Technical Data (continued)

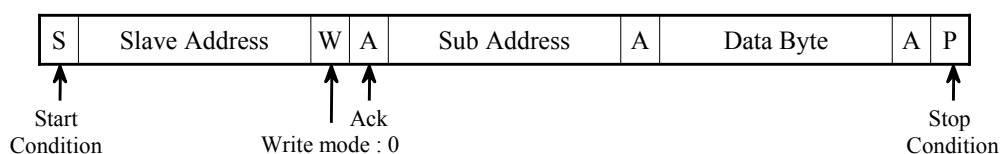
6. I²C-bus Interface (continued)

d.) Data format

Slave Address

A6	A5	A4	A3	A2	A1	A0	R/W	Hex
1	1	1	0	0	1	0	x	72h

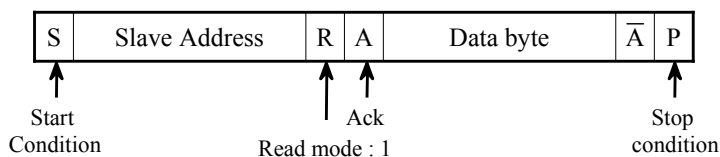
• Write mode



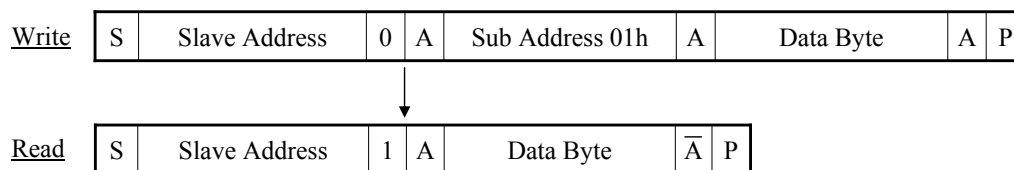
• Read mode

d1.) When Sub address is not specified

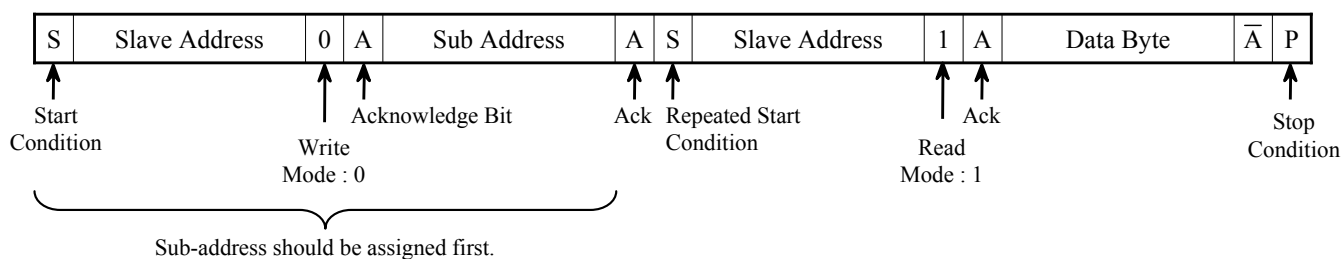
When data is read without assigning sub-address, it is possible to read the value of sub-address specified in Write mode immediately before.



Ex) When writing data into address and reading data from "01 h".



d2.) When Sub address is specified



	Product Standards	NN30295A	
		Total Pages	Page
		28	23

■ Technical Data (continued)

7. Register Map

Sub Address	R/W	Register Name	Bit	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
10h	R/W	CNT	Name	—	FSEL[2:0]			—	—	FCCM	DCDCOFF
			Default	—	0	0	0	—	—	0	0
11h	R/W	DAC	Name	—	—	—	—	VDC[3:0]			
			Default	—	—	—	—	0	0	0	0

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	Product Standards	NN30295A	
		Total Pages	Page
		28	24

■ Technical Data (continued)

7. Register map details

Sub Address	R/W	Register Name	Bit	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
10h	R/W	CNT	Name	—	FSEL[2:0]			—	—	FCCM	DCDCOFF
			Default	—	0	0	0	—	—	0	0

D6-D4 (FSEL Setting)

FSEL[6:4]			FREQUENCY (MHz)	Default
D6	D5	D4		
0	0	0	1.00	
0	0	1	0.50	
0	1	0	0.75	
0	1	1	1.00	
1	0	0	1.25	
1	0	1	1.50	
1	1	0	1.75	
1	1	1	2.00	

D1: FCCM:

0:Default(Skip Mode)
1:Force CCM Mode

D0: DCDCOFF

0:Default(DCDC On)
1:DCDC Off

	Product Standards	NN30295A	
		Total Pages	Page
		28	25

■ Technical Data (continued)

7. Register map details

Sub Address	R/W	Register Name	Bit	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
11h	R/W	DAC	Name	—	—	—	—	VDC[3:0]			
			Default	—	—	—	—	0	0	0	0

D3-0 : DCDC Output Voltage Setting Register

VDC1[3:0]				Output Voltage [V]
D3	D2	D1	D0	
0	0	0	0	1.000
0	0	0	1	0.880
0	0	1	0	0.895
0	0	1	1	0.910
0	1	0	0	0.925
0	1	0	1	0.940
0	1	1	0	0.955
0	1	1	1	0.970
1	0	0	0	0.985
1	0	0	1	1.000
1	0	1	0	1.015
1	0	1	1	1.030
1	1	0	0	1.045
1	1	0	1	1.060
1	1	1	0	1.075
1	1	1	1	1.090

Default

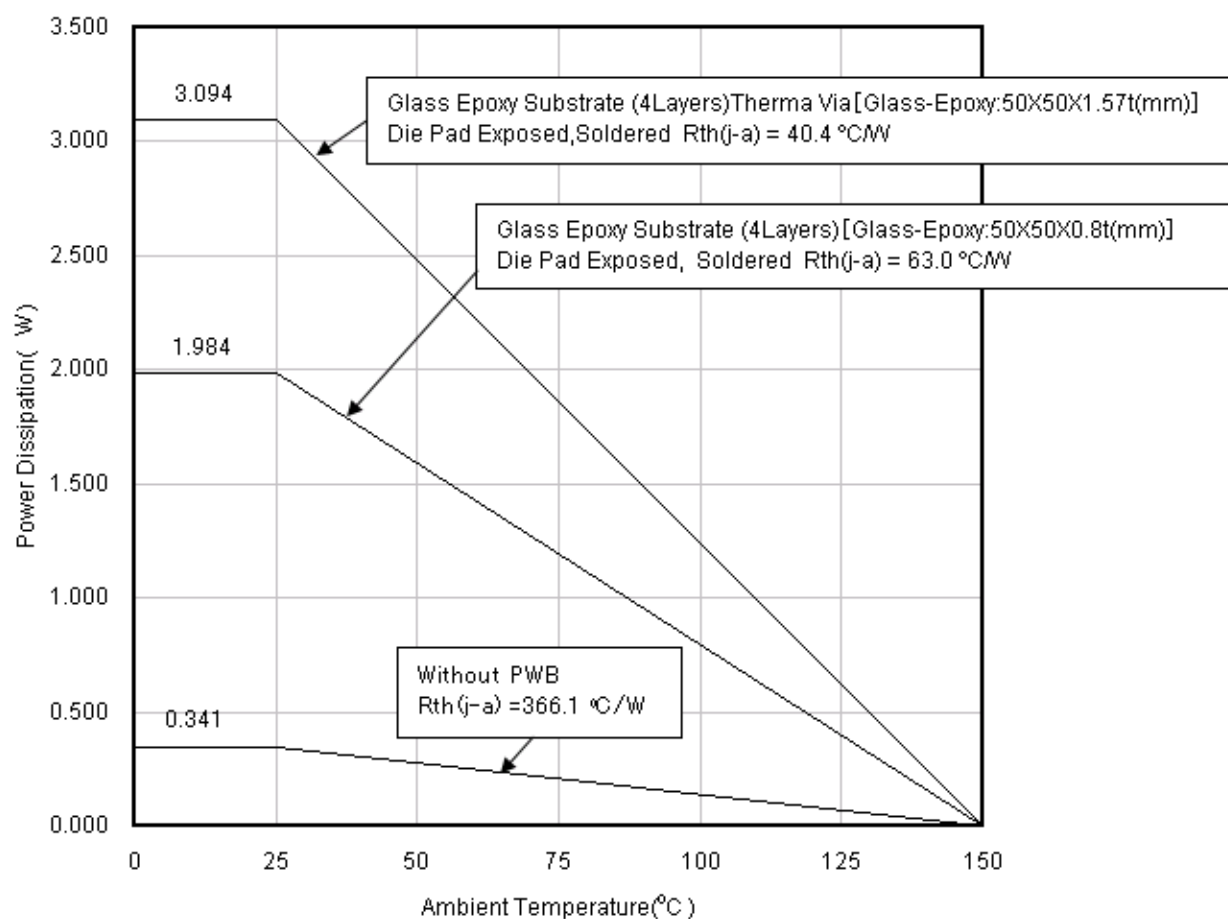
Note) The required output voltage is set by changing the DAC step by 1 bit at a time.
An interval of more than 50us is required at every bit step while changing the DAC.

	Product Standards	NN30295A	
		Total Pages	Page
		28	26

■ Usage Notes

• Attention and precaution in using

1. Power dissipation (Technical report)



Product Standards

NN30295A

Total Pages

Page

28

27

■ Usage Notes (continued)

• Attention and precaution in using (continued)

2. Power dissipation (Supplementary explanation)

[Experiment environment]

Power Dissipation (Technical Report) is a result in the experiment environment of SEMI standard conformity. (Ambient air temperature (Ta) is 25 degrees C)

[Supplementary information of PWB to be used for measurement]

The supplement of PWB information for Power Dissipation data (Technical Report) are shown below.

Indication	Total Layer	Resin Material
Glass-Epoxy	1-layer	FR-4
4-layer	4-layer	FR-4

[Notes about Power Dissipation (Thermal Resistance)]

Power Dissipation values (Thermal Resistance) depend on the conditions of the surroundings, such as specification of PWB and a mounting condition , and a ambient temperature. (Power Dissipation (Thermal Resistance) is not a fixed value.)

The Power Dissipation value (Technical Report) is the experiment result in specific conditions (evaluation environment of SEMI standard conformity) ,and keep in mind that Power Dissipation values (Thermal resistance) depend on circumference conditions and also change.

[Definition of each temperature and thermal resistance]

Ta : Ambient air temperature

※The temperature of the air is defined at the position where the convection, radiation, etc. don't affect the temperature value, and it's separated from the heating elements.

Tc : It's the temperature near the center of a package surface. The package surface is defined at the opposite side if the PWB.

Tj : Semiconductor element surface temperature (Junction temperature.)

Rth(j-c) : The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the package surface

Rth(c-a) : The thermal resistance (difference of temperature of per 1 Watts) between the package surface and the ambient air

Rth(j-a) : The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the ambient air

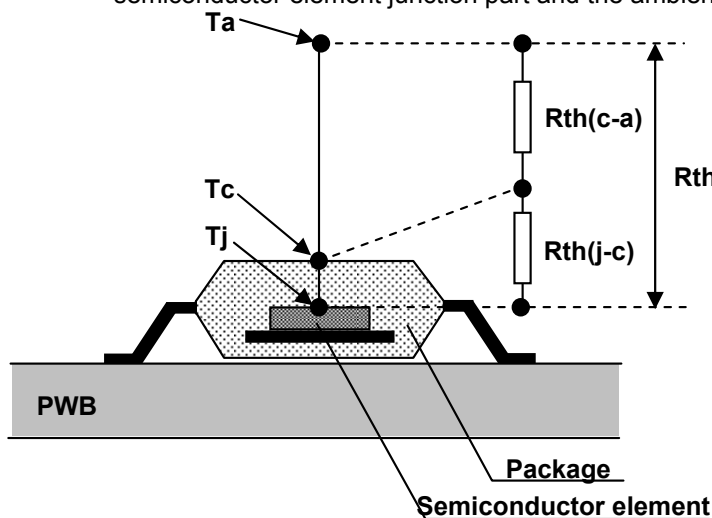


Fig1. Definition image

[Definition formula]

$$T_j = \{R_{th(j-c)} + R_{th(c-a)}\} \times P + T_a$$

$$= R_{th(j-a)} \times P + T_a$$

$$R_{th(j-c)} = \frac{T_j - T_c}{P} \quad (^\circ\text{C/W})$$

$$R_{th(c-a)} = \frac{T_c - T_a}{P} \quad (^\circ\text{C/W})$$

$$R_{th(j-a)} = \frac{T_j - T_a}{P} \quad (^\circ\text{C/W})$$

$$= R_{th(j-c)} + R_{th(c-a)}$$

P: power(W)

	Product Standards	NN30295A	
		Total Pages	Page
		28	28

■ Usage Notes (continued)

• Special attention and precaution in using

1. This IC is intended to be used for general electronic equipment.

Consult our sales staff in advance for information on the following applications:

- Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
- Any applications other than the standard applications intended.
 - (1) Space appliance (such as artificial satellite, and rocket)
 - (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
 - (3) Medical equipment for life support
 - (4) Submarine transponder
 - (5) Control equipment for power plant
 - (6) Disaster prevention and security device
 - (7) Weapon
 - (8) Others : Applications of which reliability equivalent to (1) to (7) is required

It is to be understood that our company shall not be held responsible for any damage incurred as a result of or in connection with your using the IC described in this book for any special application, unless our company agrees to your using the IC in this book for any special application.

2. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.
3. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
4. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.
5. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin- V_{CC} short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) .
And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.
6. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.
7. When using the LSI for new models, verify the safety including the long-term reliability for each product.
8. When the application system is designed by using this LSI, be sure to confirm notes in this book.
Be sure to read the notes to descriptions and the usage notes in the book.
9. Connect the metallic plates on the back side of the IC with their respective potentials (AGND, PVIN, LX). The thermal resistance and the electrical characteristics are guaranteed only when the metallic plates are connected with their respective potentials.