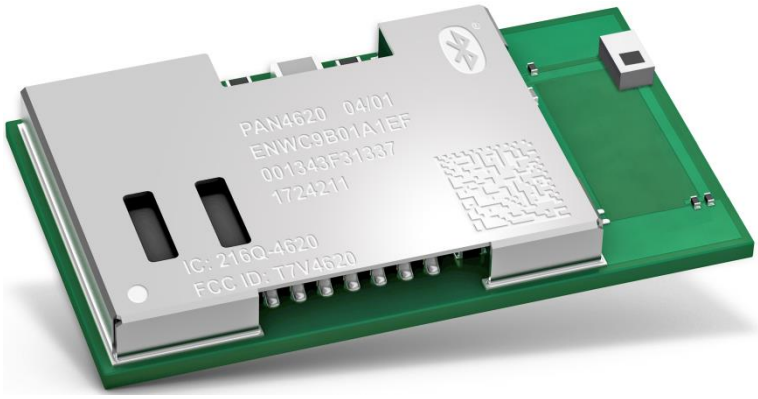
Panasonic

PAN4620

IEEE® 802.15.4 and Bluetooth® Low Energy Module

Product Specification

Rev. 1.1



Wireless Modules

Overview

The PAN4620 is Panasonic's Internet of Things dual mode module comprising the NXP® Kinetis® MKW41Z512CAT4 SoC – a 2.4 GHz 802.15.4 and Bluetooth Low Energy wireless radio microcontroller based on an ARM® Cortex® M0+.

Features

- UART, SPI, I²C, TSI, ADC, and DAC
- Same form factor and compatible pinout for VCC, GND, Reset, UART, I²C, and SWD as PAN1026, PAN1760, PAN1760A, and PAN1761
- Single and concurrent operation of IEEE 802.15.4 and Bluetooth Low Energy
- Open to various known application layers or proprietary solutions
- Surface Mount Type dimensions: 15.6 mm x 8.7 mm x 1.9 mm
- On module 32 MHz and 32 kHz crystal
- SoC: NXP Kinetis KW41Z – 2.4 GHz 802.15.4 and Bluetooth Low Energy 4.2 Wireless Radio Microcontroller
- Core: Up to 48 MHz 32 bit ARM Cortex-M0+
- Memory: 512 kB of flash and 128 kB of SRAM
- Voltage range: 1.8 V to 4.2 V
- Temperature range: -40 °C to 85 °C

Characteristics

- Transceiver frequency range 2 360 MHz to 2 483.5 MHz
- Programmable transmitter output power: -30 dBm to 3.5 dBm (Power and sensitivity measured at chip output)
- Typical receiver sensitivity Bluetooth Low Energy @1Mbps: -95 dBm
- Typical receiver sensitivity typical for IEEE Standard 802.15.4 @250 kbps: -100 dBm
- Typical transmitter current consumption 7.6 mA (6.1 mA for Tx, 0dBm, 3.6 V)
- Typical receiver current consumption 8.4 mA (6.8 mA for RX, 3.6 V)

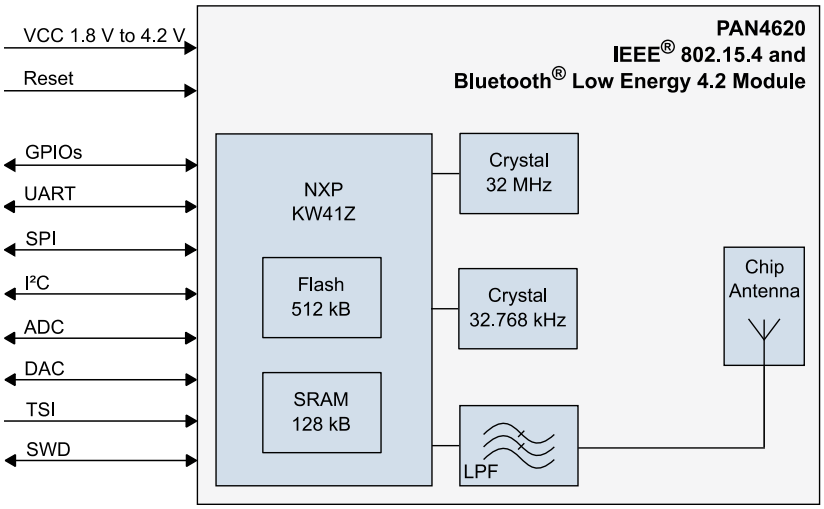
Bluetooth

- Bluetooth Low Energy 4.2 compliant implementation certified by Bluetooth SIG
- Supporting software consisting of Bluetooth Low Energy host stack and profiles and IPv6 over Bluetooth Low Energy
- Bluetooth Developer Studio Plug-In

IEEE 802.15.4

- IEEE standard 802.15.4 compliant
- Supporting software consisting of 802.15.4 MAC/PHY implementation, Simple Media Access Controller (SMAC), and the NXP certified Thread stack

Block Diagram



By purchase of any of the products described in this document the customer accepts the document's validity and declares their agreement and understanding of its contents and recommendations. Panasonic Industrial Devices Europe GmbH (Panasonic) reserves the right to make changes as required at any time without notification. Please consult the most recently issued Product Specification before initiating or completing a design.

This Product Specification does not lodge the claim to be complete and free of mistakes.

Engineering Samples (ES)

If Engineering Samples are delivered to the customer, these samples have the status “Engineering Samples”. This means that the design of this product is not yet concluded. Engineering Samples may be partially or fully functional, and they may differ from the published Product Specification.

Engineering Samples are not qualified and they are not to be used for reliability testing or series production.

Disclaimer

The customer acknowledges that samples may deviate from the Product Specification and may bear defects due to their status of development and the lack of qualification mentioned above.

Panasonic rejects any liability or product warranty for Engineering Samples. In particular, Panasonic disclaims liability for damages caused by:

- The use of the Engineering Sample other than for evaluation purposes, particularly the installation or integration in another product to be sold by the customer,
- Deviation or lapse in function of the Engineering Sample,
- Improper use of the Engineering Sample.

Panasonic Industrial Devices Europe GmbH disclaims any liability for consequential and incidental damages. In case of any queries regarding the Engineering Samples, please contact your local sales partner or the related product manager.

Table of Contents

1 About This Document

1.1 Purpose and Audience

This Product Specification provides details on the functional, operational, and electrical characteristics of the Panasonic PAN4620 module. It is intended for hardware design, application, and Original Equipment Manufacturers (OEM) engineers. The product is referred to as “the PAN4620” or “the module” within this document.

1.2 Revision History

Revision	Date	Modifications/Remarks
1.0	2018-12-07	First version
1.1	2019-07-17	Added certification information. Formatting changes.

1.3 Use of Symbols

Symbol	Description
	**Note** Indicates important information for the proper use of the product. Non-observance can lead to errors.
	**Attention** Indicates important notes that, if not observed, can put the product’s functionality at risk.
⇨ [chapter number] [chapter title]	**Cross reference** Indicates cross references within the document. **Example:** Description of the symbols used in this document ⇨ 1.3 Use of Symbol.

1.4 Related Documents

Please refer to the Panasonic website for related documents ⇨ 7.3.2 Product Information.

For further information please also refer to the datasheet and reference manual “MKW41Z512CAT4” from the NXP website.

2 Overview

The PAN4620 is Panasonic's Internet of Things dual mode module comprising the NXP Kinetis MKW41Z512CAT4 SoC – a 2.4 GHz 802.15.4 and Bluetooth Low Energy wireless radio microcontroller based on an ARM Cortex-M0+.

To provide maximum flexibility, the module can be operated in stand-alone and hosted mode. With 512 kB flash memory and 128 kB SRAM the PAN4620 can easily be used as a stand-alone controller eliminating the need for an external processor, saving complexity, space and cost. It is thus well suited for very small and low power applications. Also the integration of 802.15.4 and/or Bluetooth Low Energy connectivity into existing applications can easily be achieved when using the PAN4620 in hosted mode.

Using the PAN4620 with low power consumption in combination with the NXP certified Thread stack, Bluetooth Low Energy stack or a combination of both for concurrent operation allows to meet IoT application requirements without the need for a gateway. Since Thread does not define an application layer, various application layers can be used, such as Dotdot, IoTivity, OpenDOF, and others.

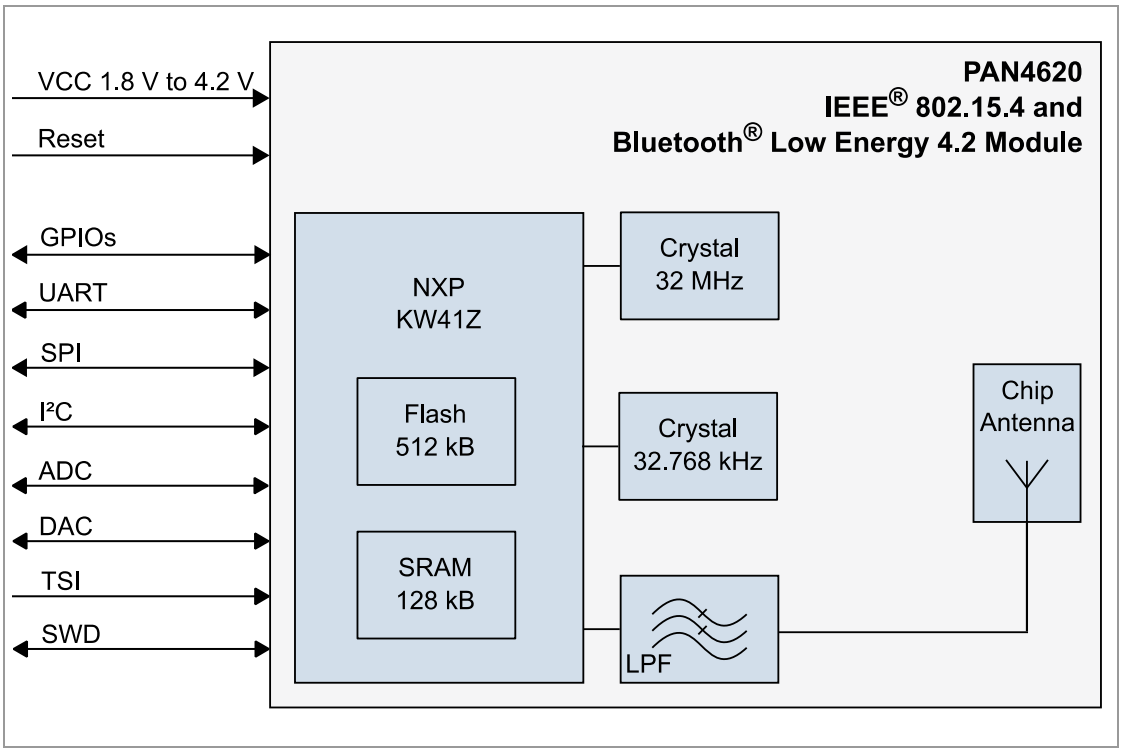
FCC, IC, and CE approval are available.

Please refer to the Panasonic website for related documents ⇨ 7.3.2 Product Information.

Further information on the variants and versions ⇨ 7.1 Ordering Information.

For further information please also refer to the datasheet MKW41Z512CAT4 and reference manual from www.nxp.com.

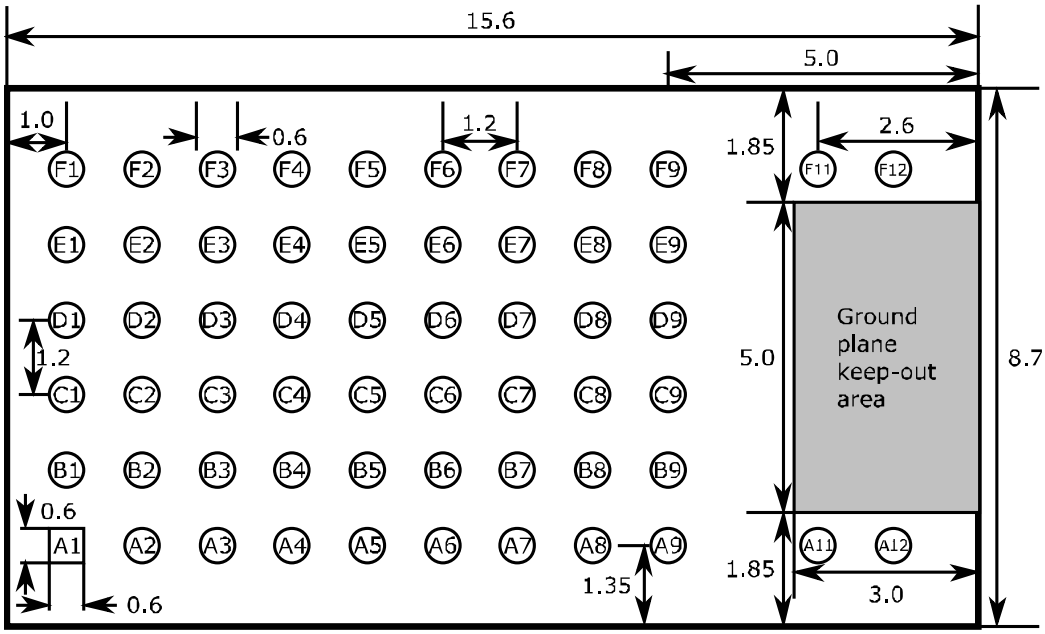
2.1 Block Diagram



2.2 Pin Configuration

Pin Assignment

Top view (dimensions are in mm)



Pin Functions

No.	Pin Name	Alternative Pin Function	Pin Type	Description
A1	GND		Ground	Connect to ground
A2	NC			Do not connect
A3	$\overline{\text{RESET}}$	PTA2, TPM0_CH3	Digital I/O	Can be configured to use the mentioned alternative pin functions
A4	NC			Do not connect
A5	VCC		Power	Supply voltage 1.8 V to 4.2 V
A6	VCC		Power	Supply voltage 1.8 V to 4.2 V
A7	GND		Ground	Connect to ground
A8	PTC18	TSI0_CH6, LLWU_P2, SPI0_SIN, I2C1_SDA, LPUART0_TX, BSM_DATA, DTM_TX	Digital I/O	Can be configured to use the mentioned alternative pin functions.

No.	Pin Name	Alternative Pin Function	Pin Type	Description
A9	GND		Ground	Connect to ground
A11	GND		Ground	Connect to ground
A12	GND		Ground	Connect to ground
B1	NC			Do not connect
B2	PTA17	TSI0_CH11, LLWU_P5, RF_RESET, SPI1_SIN, TPM_CLKIN1	Digital I/O	Can be configured to use the mentioned alternative pin functions
B3	PTC19	TSI0_CH7, LLWU_P3, SPI0_PCS0, I2C0_SCL, LPUART0_CTS_b, BSM_CLK, BLE_RF_ACTIVE	Digital I/O	Can be configured to use the mentioned alternative pin functions
B4	PTC17	TSI0_CH5, LLWU_P1 SPI0_SOUT, I2C1_SCL LPUART0_RX, BSM_FRAME, DTM_RX	Digital I/O	Can be configured to use the mentioned alternative pin functions
B5	PTC16	TSI0_CH4, LLWU_P0, SPI0_SCK, I2C0_SDA, LPUART0_RTS_b, TPM0_CH3	Digital I/O	Can be configured to use the mentioned alternative pin functions
B6	PTA16	TSI0_CH10, LLWU_P4, SPI1_SOUT, TPM0_CH0	Digital I/O	Can be configured to use the mentioned alternative pin functions.
B7	NC			Do not connect
B8	NC			Do not connect
B9	NC			Do not connect
C1	NC			Do not connect
C2	PTA19	TSI0_CH13, ADC0_SE5, LLWU_P7, SPI1_PCS0, TPM2_CH1	Digital I/O	Can be configured to use the mentioned alternative pin functions
C3	PTA18	TSI0_CH12, LLWU_P6, SPI1_SCK, TPM2_CH0	Digital I/O	Can be configured to use the mentioned alternative pin functions
C4	SWDIO	PTA0, TSI0_CH8, SPI0_PCS1, TPM1_CH0, SWD_DIO	Digital I/O	Can be configured to use the mentioned alternative pin functions.
C5	SWDCLK	PTA1, TSI0_CH9, SPI1_PCS0, TPM1_CH1, SWD_CLK	Digital I/O	Can be configured to use the mentioned alternative pin functions.

No.	Pin Name	Alternative Pin Function	Pin Type	Description
C6	PTC1	I2C0_SDA, LPUART0_RTS_b, TPM0_CH2, BLE_RF_ACTIVE	Digital I/O	Can be configured to use the mentioned alternative pin functions.
C7	NC			Do not connect
C8	GND		Ground	Connect to ground
C9	GND		Ground	Connect to ground
D1	PTB0	LLWU_P8, XTAL_OUT_EN, I2C0_SCL, CMP0_OUT, TPM0_CH1, CLKOUT	Digital I/O	Can be configured to use the mentioned alternative pin functions.
D2	PTB1	ADC0_SE1, CMP0_IN5, DTM_RX, I2C0_SDA, LPTMR0_ALT1, TPM0_CH2, CMT_IRO	Digital I/O	Can be configured to use the mentioned alternative pin functions.
D3	PTB2	ADC0_SE3, CMP0_IN3, RF_NOT_ALLOWED, DTM_TX, TPM1_CH0	Digital I/O	Can be configured to use the mentioned alternative pin functions.
D4	PTB3	ADC0_SE2, CMP0_IN4, CLKOUT, TPM1_CH1, RTC_CLKOUT	Digital I/O	Can be configured to use the mentioned alternative pin functions.
D5	NC			Do not connect
D6	NC			Do not connect
D7	GND		Ground	Connect to ground
D8	GND		Ground	Connect to ground
D9	NC (ANT)			This pad is not connected, but by moving a jumper (0201 size) on the module, it can be used as RF bottom pad for testing purposes.
E1	PTC3	TSI0_CH15, LLWU_P11, RX_SWITCH, I2C1_SDA, LPUART0_TX, TPM0_CH1, DTM_TX	Digital I/O	Can be configured to use the mentioned alternative pin functions.
E2	PTC2	TSI0_CH14, LLWU_P10, TX_SWITCH, I2C1_SCL, LPUART0_RX, CMT_IRO, DTM_RX	Digital I/O	Can be configured to use the mentioned alternative pin functions.
E3	NC			Do not connect

No.	Pin Name	Alternative Pin Function	Pin Type	Description
E4	NC			Do not connect
E5	PTC0	LLWU_P9, I2C0_SCL, LPUART0_CTS_b, TPM0_CH1	Digital I/O	Can be configured to use the mentioned alternative pin functions.
E6	PTC6	TSI0_CH2, LLWU_P14, XTAL_OUT_EN, I2C1_SCL, LPUART0_RX, TPM2_CH0, BSM_FRAME	Digital I/O	Can be configured to use the mentioned alternative pin functions.
E7	VREFH/_OUT		O	Internally generated voltage reference output
E8	GND		Ground	Connect to ground
E9	GND		Ground	Connect to ground
F1	GND		Ground	Connect to ground
F2	NC			Do not connect
F3	ADC0_DP0, CMP0_IN0		Analog	
F4	ADC0_DM0, CMP0_IN1		Analog	
F5	PTC4	TSI0_CH0, LLWU_P12, LPUART0_CTS_b, TPM1_CH0, BSM_DATA	Digital I/O	Can be configured to use the mentioned alternative pin functions.
F6	PTB18	DAC0_OUT, ADC0_SE4, CMP0_IN2, I2C1_SCL, TPM_CLKIN0, TPM0_CH0	Digital I/O	Can be configured to use the mentioned alternative pin functions.
F7	PTC7	TSI0_CH3, LLWU_P15, SPI0_PCS2, I2C1_SDA, LPUART0_TX, TPM2_CH1, BSM_DATA	Digital I/O	Can be configured to use the mentioned alternative pin functions.
F8	PTC5	TSI0_CH1, LLWU_P13, RF_NOT_ALLOWED LPTMR0_ALT2, LPUART0_RTS_b, TPM1_CH1, BSM_CLK	Digital I/O	Can be configured to use the mentioned alternative pin functions.
F9	GND		Ground	Connect to ground
F11	GND		Ground	Connect to ground
F12	GND		Ground	Connect to ground

2.3 Transceiver Features

The PAN4620 features an integrated chip antenna and corresponding matching networks.

Both, a high accuracy 32 MHz crystal and a low frequency clock are integrated in the module. Therefore, no external crystal is required to make full use of the reduced power modes.

The operating frequency is in the ISM band and the MBAN band from 2 360 MHz to 2 483.5 MHz with a programmable output power from -30 dBm to 3.5 dBm

2.3.1 Bluetooth Features

- Bluetooth Low Energy 4.2 (1 Mbps)
- Two simultaneous connections (2 independent hardware connection engines)
- Receive sensitivity of -95 dBm

For further information see ⇨ 4.9 Transceiver Feature Summary.

2.3.2 IEEE 802.15.4 Features

- IEEE Standard 802.15.4-2011 compliant OQPSK modulation
- Receive sensitivity of -100 dBm (Receive sensitivity in generic FSK modes depends on mode selection and data rate.)
- Hardware acceleration for packet processing/link layer
- NXP certified Thread stack

For further information see ⇨ 4.9 Transceiver Feature Summary.

2.3.3 MCU Features

The KW41Z features an ARM Cortex-M0+MCU with up to 48 MHz. As compared to Cortex-M0, the Cortex-M0+ uses optimized 2-stage pipeline microarchitecture for reduced power consumption and improved architectural performance (cycles per instruction).

Interrupt Controller

- Supports up to 32 interrupt request sources
- 32 vectored interrupts, 4 programmable priority levels
- Includes a single non-maskable interrupt
- Supports interrupt handling when system clocking is disabled in low power modes.

On Chip Memory

- 512 kB flash memory implemented as two equal 256 kB blocks.
- One block can be read or erased, while code is being executed or read from another.

- Flash can be marked execute only in 8 kB blocks to prevent code from being read by third parties.
- 128 kB SRAM
- The chip features security circuitry to prevent unauthorized access to RAM and flash contents through the debugger.

Debug Controller

- Serial wire debug (SWD) interface
- Hardware breakpoint unit for two code addresses
- Hardware watchpoint unit for two data items
- Micro trace buffer for program tracing

2.3.4 Security Features

- Advanced encryption standard accelerator (AES-128 Accelerator)
- True random number generator (TRNG)
- Flash memory protection

2.3.5 Power Management Control Unit

- Supports external voltage sources of 1.8 V to 4.2 V (2.1 V required for startup) and is therefore ideally suited for single coin-cell battery operation.
- Programmable power saving modes
- Integrated low frequency clock to make full use of the reduced power modes
- Available wake-up from power saving modes via internal and external sources
- Integrated power-on reset (POR)
- Integrated low voltage detect (LVD) with reset (brownout) capability
- Selectable LVD trip points
- Programmable low voltage warning (LVW) interrupt capability
- Individual peripheral clocks can be gated off to reduce current consumption
- Internal buffered bandgap reference voltage
- Factory programmed trim for bandgap and LVD
- 1 kHz low power oscillator (LPO)

2.3.6 Peripheral Features

- 16-Bit analog-to-digital converter
- 12-Bit digital-to-analog converter
- High-speed analog comparator (CMP)
- Timer: low power timer (LPTMR), timer/PWM, programmable interrupt timer (PIT),

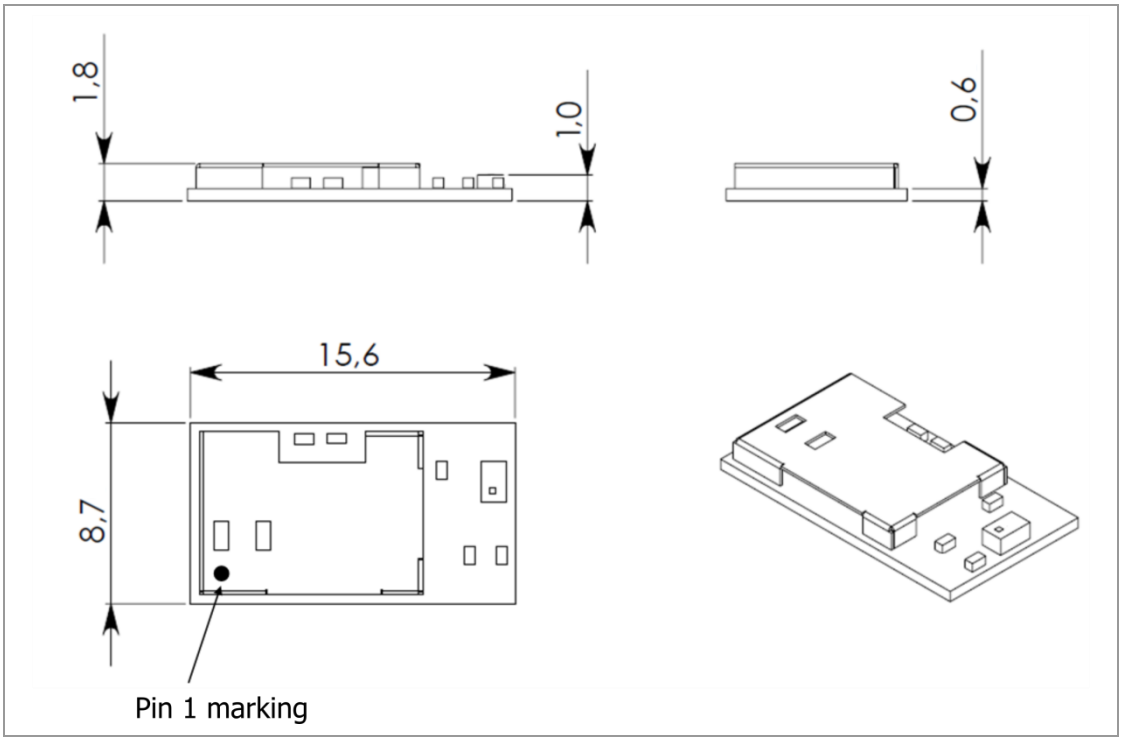
- Real-time clock (RTC)
- Inter-integrated circuit (I²C), two channels, up to 400 kHz, multi-master operation
- Low power universal asynchronous receiver transmitter (LPUART), one channel full-duplex operation
- Serial peripheral interface (SPI), master and slave mode, full-duplex, three-wire synchronous transfers
- Carrier modulator timer (CMT) with four modes of operation
- Touch sensor input (TSI) with up to 16 external electrodes
- 24 General purpose Input/Outputs
- GPIOs can be configured to function as a interrupt driven keyboard scanning matrix

For further information see ⇨ 4.6 Interface Specification.

3 Detailed Description

3.1 Dimensions

All dimensions are in millimeters.

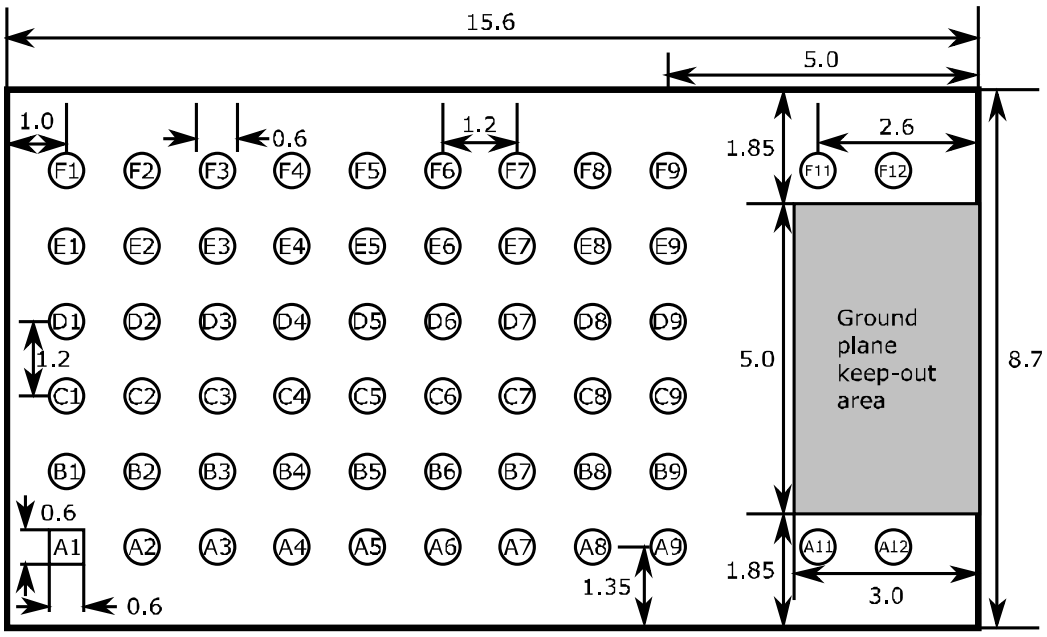


No.	Item	Dimension	Tolerance	Remark
1	Width	8.70	± 0.35	
2	Length	15.60	± 0.35	
3	Height	1.80	± 0.35	With case

3.2 Footprint

The outer dimensions have a tolerance of ±0.35 mm.

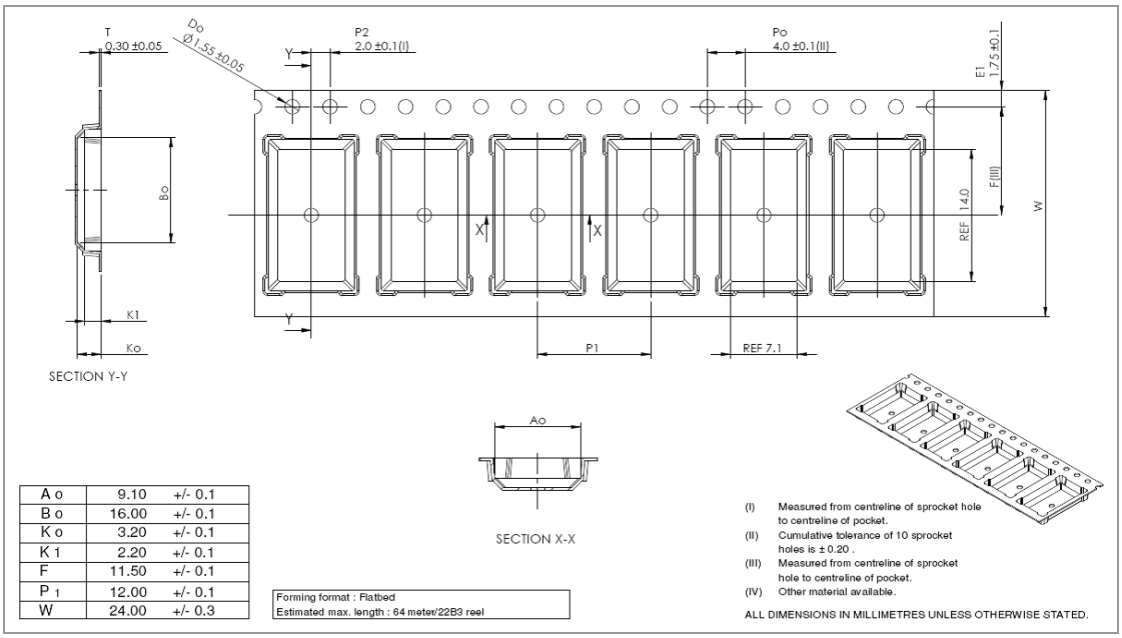
Top view (dimensions are in mm)



3.3 Packaging

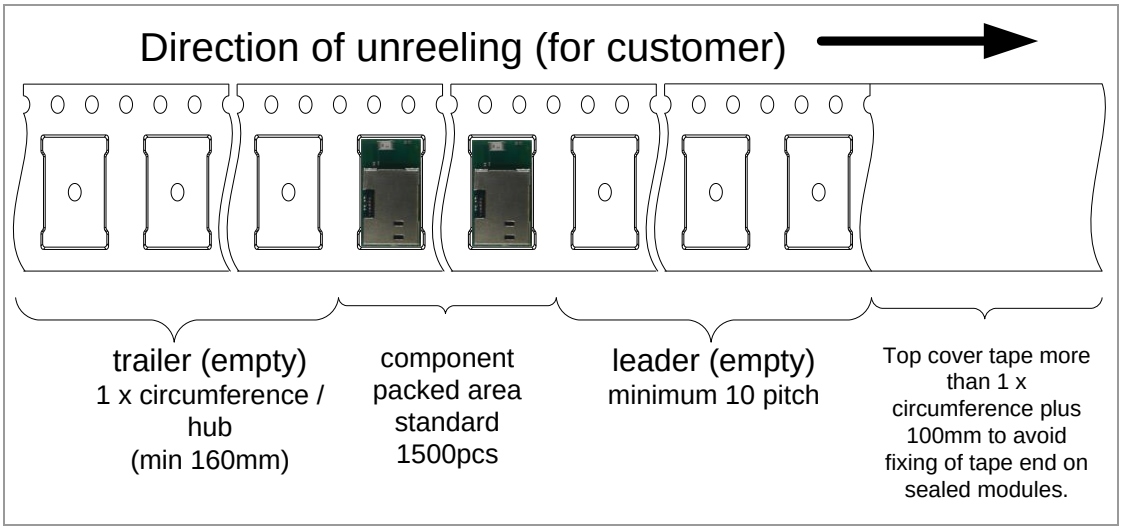
The product is an engineering sample status product and will be delivered in the package described below.

3.3.1 Tape Dimensions



A o	9.10	+/- 0.1
B o	16.00	+/- 0.1
K o	3.20	+/- 0.1
K 1	2.20	+/- 0.1
F	11.50	+/- 0.1
P 1	12.00	+/- 0.1
W	24.00	+/- 0.3

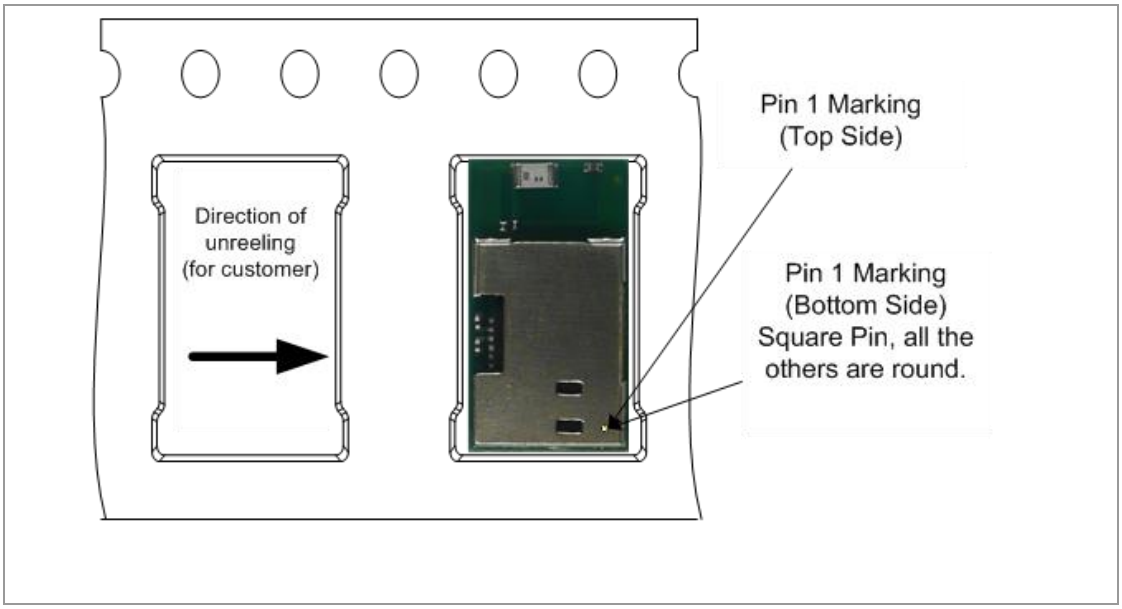
3.3.2 Packing in Tape



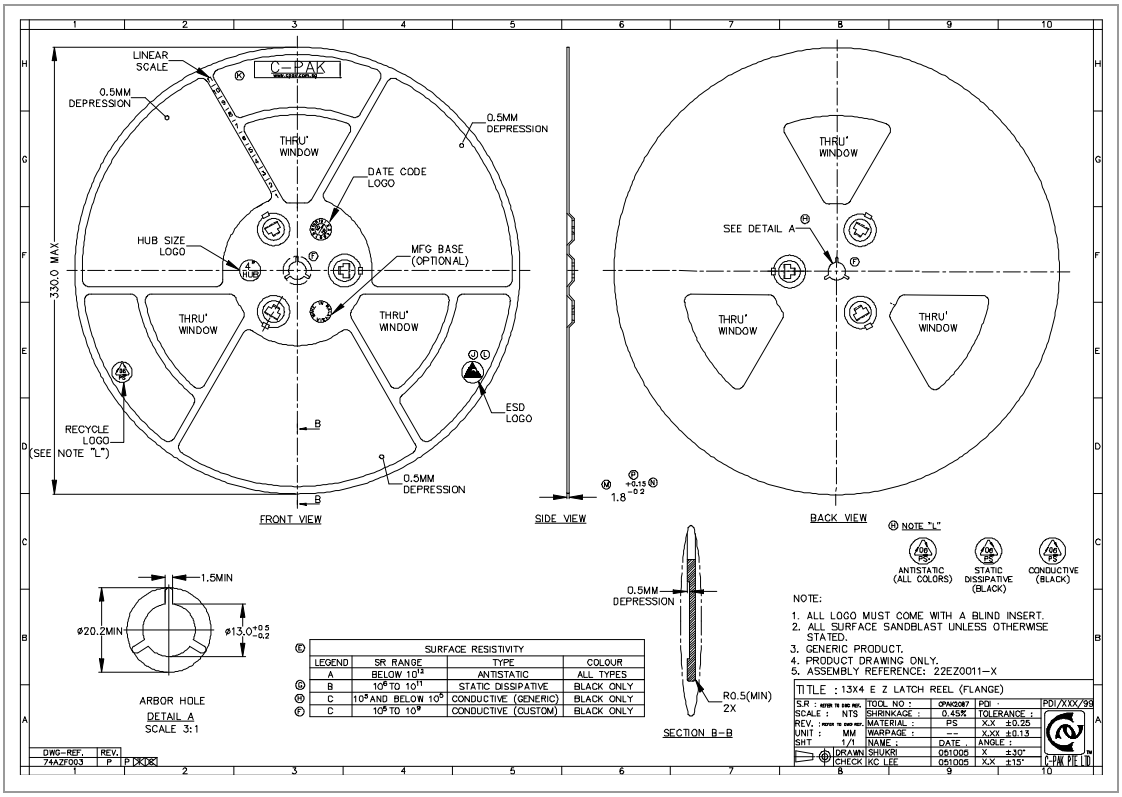
Empty spaces in the component packed area shall be less than two per reel and those spaces shall not be consecutive.

The top cover tape shall not be found on reel holes and it shall not stick out from the reel.

3.3.3 Component Direction

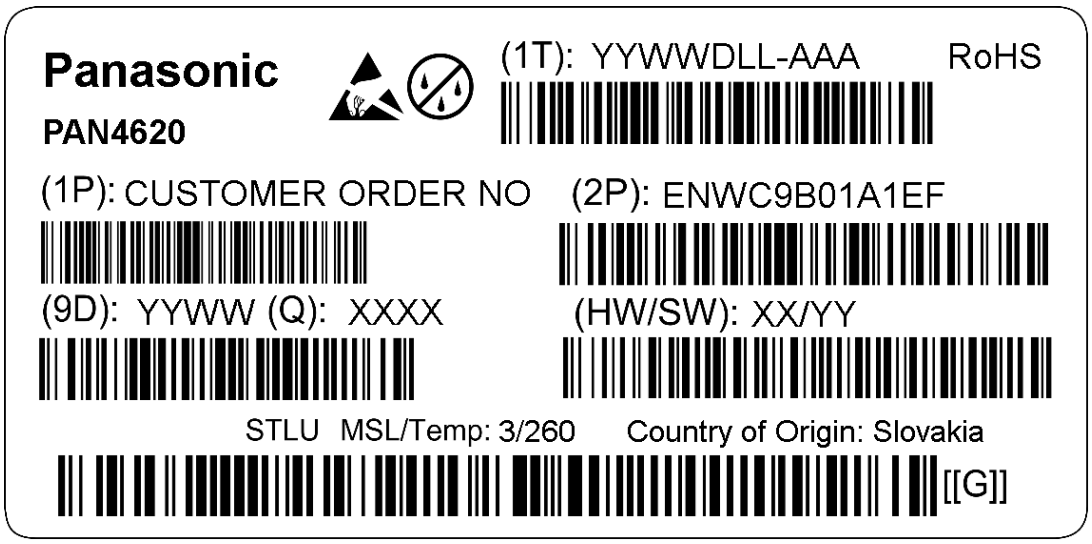


3.3.4 Reel Dimension



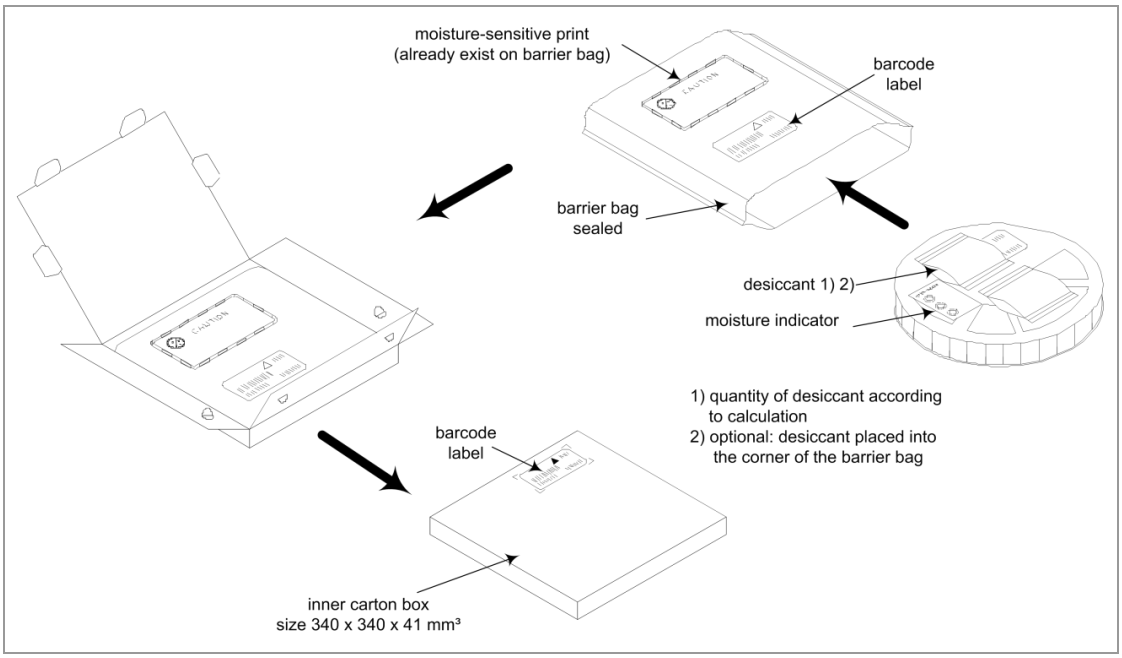
SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{4}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{3} AND BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
C	10^{5} TO 10^{9}	CONDUCTIVE (CUSTOM)	BLACK ONLY

3.3.5 Package Label

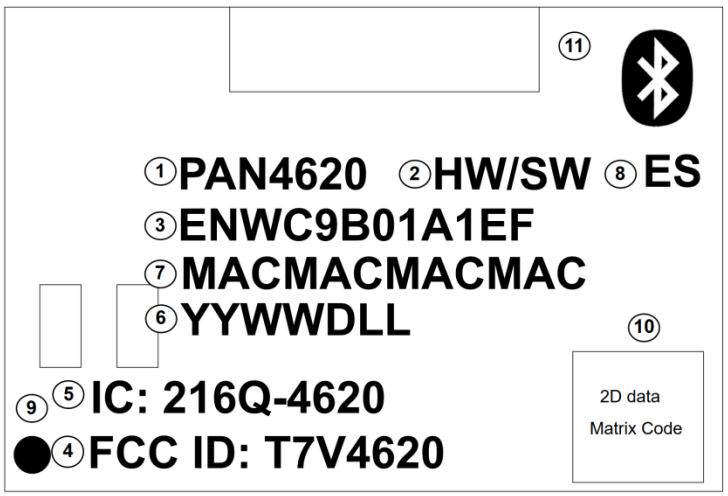


(1T)	Lot code
(1P)	Customer order number, if applicable
(2P)	Order number
(9D)	Date code
(Q)	Quantity
(HW/SW)	Hardware/software version

3.3.6 Total Package



3.4 Case Marking



1	Brand name
2	Hardware/Software Version
3	ENW-No./Model Name
4	FCC ID
5	IC ID
6	Lot code
7	MAC address (EUI-48)
8	Engineering Sample marking, if applicable
9	Marking for Pin 1
10	2D barcode for internal usage only
11	Bluetooth logo

3.5 Production Data Storage

The production data consists of the Extended Unique Identifier EUI-48 the EUI-64, and the crystal trim value. The information is stored in the last sector of the flash, which starts at 0x7F800.

The short EUI-48 is stored at 0x7f832 and is also, as described in ⇨ 3.4 Case Marking, lasered on the module cover. If the last flash sector is erased by accident, the EUI-48 can be recovered from the cover.

The extended address EUI-64 is stored at 0x7f82a and it is constructed from the EUI-48. A block FFFE is inserted between the Organizationally Unique Identifier (OUI) (fixed Panasonic identifier) and the rest of the address.

Example

001343AABBCC – EUI-48 (Written on the cover)

001343FFFEAABBCC – EUI-64 (Constructed from the short address)

The 1 byte crystal trim value is optimized during the production test for each module and saved at 0x7F838. If this value is deleted by accident, a default of 0x30 should be used.

4 Specification

All specifications are over temperature and process, unless indicated otherwise.

4.1 Default Test Conditions

Temperature:	25 ± 10 °C
Humidity:	40 to 85 % RH
Supply Voltage:	3.6 V

4.2 Absolute Maximum Ratings

The maximum ratings may not be exceeded under any circumstances, not even momentarily or individually, as permanent damage to the module may result.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{STOR}	Storage Temperature		-40		+85	°C
V_{ESD}	ESD robustness	Electrostatic discharge voltage, human body model	-2 000		+2 000	V
		Electrostatic discharge voltage, charged-device model	-500		+500	
RF input power	P_{max}				10	dBm
V_{DD}	Supply voltage		-0.3		4.2	V
V_{IO}	Voltage on any IO pin		-0.3		V_{DD}+0.3	V

4.3 Recommended Operating Conditions

The maximum ratings may not be exceeded under any circumstances, not even momentarily or individually, as permanent damage to the module may result.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	DCDC converter needs this minimum voltage to start.	2.1		4.2	V
		The supply can drop to this minimum voltage after DCDC converter settles.	1.8[1]			
f_{IN}	Input frequency		2.36		2.48	GHz
T_A	Ambient temperature range		-40	25	75	°C
V_{IO}	Voltage on any IO pin		-0.3		V_{DD}+0.3	V
I_D	Instantaneous max. current	Single pin limit (applies to all port pins)	-25		25	mA
V_{IL}	Logic low input voltage		0		0.3·$V_{DD\,INT}$[2]	V
V_{IH}	Logic high input voltage		0.7·$V_{DD\,INT}$		$V_{DD\,INT}$	V

4.4 Current Consumption

The current consumption depends on the user scenario and on the setup and timing in the power modes.

Assume V_{DD}=3.6 V, T_{amb}=25 °C, if nothing else is stated.

[1] DC-DC converter requires slightly higher input voltage during startup. Bit DCDC_STS_DC_OK will be set when the DC-DC converter finished the startup sequence. Typical startup time is 50 ms and it varies with the loading of the converter.

[2] $V_{DD\,INT}$ is the internal LDO regulated voltage supplying various circuit blocks, $V_{DD\,INT}$=1.2 V.

Parameter	Condition	Min.	Typ.	Max.	Unit
Typical average RX current	Measured under continuous RX with MCU stop/Flash doze		8.4		mA
Typical average TX (0 dBm) current	Measured under continuous TX with MCU stop/Flash doze		7.6		mA
Typical average RX current	Measured under continuous RX with MCU run/Flash enabled		10.2		mA
Typical average TX (0 dBm) current	Measured under continuous TX with MCU run/Flash enabled		9.6		mA
Low Power Mode current	Current consumption in very low leakage stop mode VLLS1		0.67	1.07	µA

4.5 Internal Operating Frequencies

Symbol	Parameter	Condition	Max.	Unit
f_{SYS}	System and core clock	Normal run mode	48	MHz
f_{BUS}	Bus clock	Normal run mode	24	
f_{FLASH}	Flash clock			
f_{LPTMR}	LPTMR clock			
f_{SYS}	System and core clock	VLPR and VLPS mode	4	
f_{BUS}	Bus clock	VLPR and VLPS mode[3]	1	
f_{FLASH}	Flash clock			
f_{LPTMR}	LPTMR clock[4]	VLPR and VLPS mode[3]	24	
f_{ERCLK}	External reference clock	VLPR and VLPS mode[3]	16	
$f_{LPTMR-ERCLK}$	LPTMR external reference clock			
f_{TPM}	TPM asynchronous clock	VLPR and VLPS mode[3]	8	
$f_{LPUART0}$	LPUART0 asynchronous clock	VLPR and VLPS mode[3]	12	

4.6 Interface Specification

4.6.1 LPUART

See also ⇨ 4.8 General Switching Specification.

Signal Name	Description	I/O	Pad
LPUART0_RX	Receive data	I	B4, E2, E6
LPUART0_TX	Transmit data	I/O	A8, E1, F7

[3] The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.

[4] The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

Signal Name	Description	I/O	Pad
LPUART0_CTS_b	Clear to send	I	B3, E5, F5
LPUART0_RTS_b	Request to send	O	B5, C6, F8

Description	Range	Default
Baud rate	Programmable baud rates (13-bit modulo divider)	115 200
Data bits	Programmable 8-bit or 9-bit data format	8 data bits
Parity bits	Hardware parity generation and checking	No parity
Stop bit	1-2	One stop bit

4.6.2 Inter-Integrated Circuit (I^2C)

Two I^2C channels

See also ⇨ 4.8 General Switching Specification.

Signal Name	Module	Description	I/O	Pad
I2C0_SCL	I2C0	I^2C serial clock line	I/O	B3, D1, E5
I2C0_SDA	I2C0	I^2C serial data line	I/O	B5, C6, D2
I2C1_SCL	I2C1	I^2C serial clock line	I/O	B4, E2, E6
I2C1_SDA	I2C1	I^2C serial data line	I/O	A8, E1, F7

I^2C timing

Compare ⇨ Figure 1.

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
t_{HD}; STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4	-	0.6	-	µs
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock	4	-	0.6	-	µs
t_{SU}; STA	Set-up time for a repeated START condition	4.7	-	0.6	-	µs
t_{HD}; DAT	Data hold time for I^2C bus devices	0[5]	3.45[6]	0[7]	0.9[6]	µs

[5] The master mode I^2C deassert ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.

[6] The maximum t_{HD}; DAT must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

[7] Input signal Slew=10 ns and Output Load=50 pF.

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
t_{SU}; DAT	Data set-up time	250[8]	-	100[6,9]	-	ns
t_r	Rise time of SDA and SCL signals	-	1 000	$20+0.1C_b$[10]	300	ns
t_f	Fall time of SDA and SCL signals	-	300	$20+0.1C_b$[9]	300	ns
t_{SU}; STO	Set-up time for STOP condition	4	-	0.6	-	µs
t_{BUF}	Bus free time between STOP and START condition	4.7	-	1.3	-	µs
t_{SP}	Width of spikes that must be suppressed by the input filter	N/A	N/A	0	50	µs

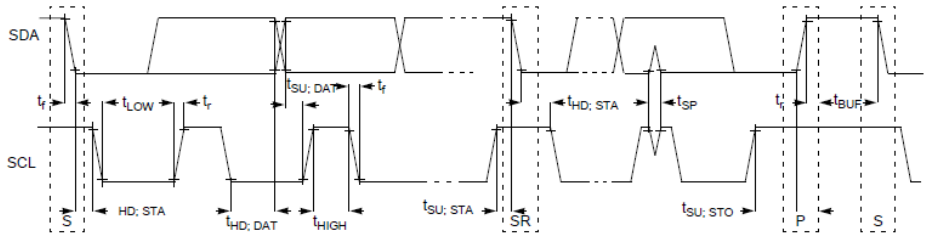


Figure 1: Timing definition for fast and standard mode devices on the I^2C bus.

[8] Set-up time in slave-transmitter mode is 1 IPbus clock period, if the TX FIFO is empty.

[9] A Fast mode I^2C bus device can be used in a Standard mode I^2C bus system, but the requirement t_{SU}; DAT≥250 ns must then be met. This is automatically the case, if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal then it must output the next data bit to the SDA line t_{rmax} + t_{SU}; DAT=1 000+250=1 250 ns (according to the Standard mode I^2C bus specification), before the SCL line is released.

[10] C_b=total capacitance of the one bus line in pF.

4.6.3 DMA Serial Peripheral Interface (DSPI)

Two independent SPI channels Master/Slave

Signal Name	Module	Description	I/O	Pad
SPI0_PCS0	SPI0	Chip Select/Slave Select	I/O	B3
SPI0_PCS1	SPI0	Chip Select	O	C4
SPI0_PCS2	SPI0	Chip Select	O	F7
SPI0_SCK	SPI0	Serial Clock	I/O	B5
SPI0_SIN	SPI0	Data In	I	A8
SPI0_SOUT	SPI0	Data Out	O	B4
SPI1_PCS0	SPI1	Chip Select/Slave Select	I/O	B3
SPI1_SCK	SPI1	Serial Clock	I/O	C3
SPI1_SIN	SPI1	Data In	I	B2
SPI1_SOUT	SPI1	Data Out	O	B6

4.6.3.1 DSPI Switching Specifications (Limited Voltage Range)

Master mode DSPI timing

Compare ⇨ Figure 2.

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation	-	12	MHz
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	-	ns
DS2	DSPI_SCK output high/low time	(t_{SCK}/2)-2	(t_{SCK}/2)+2	ns
DS3	DSPI_PCSn valid to DSPI_SCK delay[11]	(t_{BUS} x 2)-2	-	ns
DS4	DSPI_SCK to DSPI_PCSn invalid delay[12]	(t_{BUS} x 2)-2	-	ns
DS5	DSPI_SCK to DSPI_SOUT valid	-	8.5	ns
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	-	ns
DS7	DSPI_SIN to DSPI_SCK input setup	16.2	-	ns
DS8	DSPI_SCK to DSPI_SIN input hold	0	-	ns

[11] The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].

[12] The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

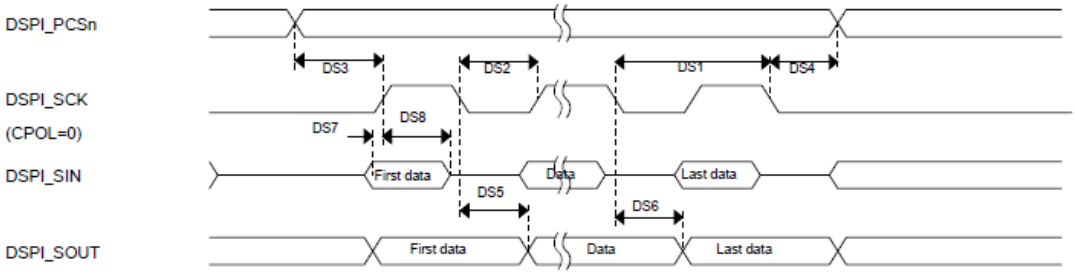


Figure 2: Master mode DSPI timing.

Slave mode DSPI timing

Compare ⇨ Figure 3.

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation	-	6	MHz
DS9	DSPI_SCK output cycle time	4 x t_{BUS}	-	ns
DS10	DSPI_SCK output high/low time	(t_{SCK}/2)-2	(t_{SCK}/2)+2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	-	21.4	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	-	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.6	-	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	-	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	-	14	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	-	14	ns

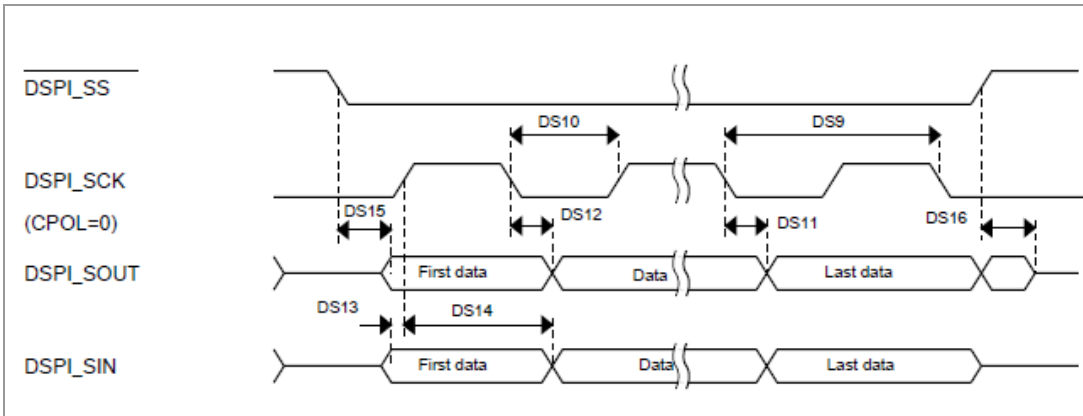


Figure 3: Slave mode DSPI timing.

4.6.3.2 DSPI Switching Specifications (Full Voltage Range)

Master mode DSPI timing

Compare ⇨ Figure 4.

Symbol	Description	Min.	Max.	Unit
	Operating voltage[13]	1.71	3.6	V
	Frequency of operation	-	12	MHz
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	-	ns
DS2	DSPI_SCK output high/low time	(t_{SCK}/2)-4	(t_{SCK}/2)+4	ns
DS3	DSPI_PCSn valid to DSPI_SCK delay[14]	(t_{BUS} x 2)-4	-	ns
DS4	DSPI_SCK to DSPI_PCSn invalid delay[15]	(t_{BUS} x 2)-4	-	ns
DS5	DSPI_SCK to DSPI_SOUT valid	-	10	ns
DS6	DSPI_SCK to DSPI_SOUT invalid	-1.2	-	ns
DS7	DSPI_SIN to DSPI_SCK input setup	23.3	-	ns
DS8	DSPI_SCK to DSPI_SIN input hold	0	-	ns

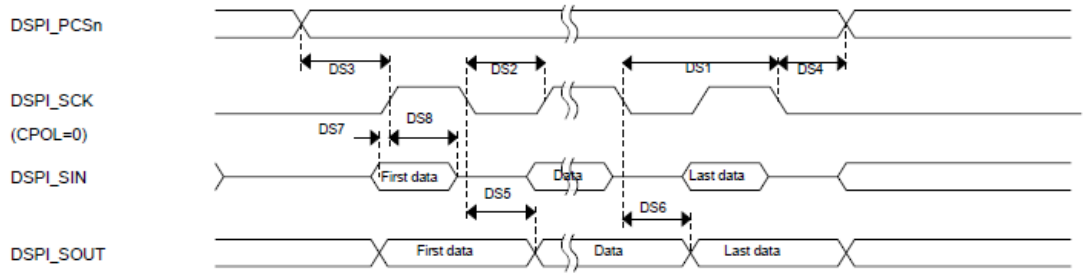


Figure 4: Master mode DSPI timing.

Slave mode DSPI timing

Compare ⇨ Figure 5.

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	-	6	MHz
DS9	DSPI_SCK output cycle time	4 x tBUS	-	ns
DS10	DSPI_SCK output high/low time	(tSCK/2)-4	(tSCK/2)+4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	-	29.1	ns

[13]The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.

[14]The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].

[15]The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

Symbol	Description	Min.	Max.	Unit
DS12	DSPI_SCK to DSPI_SOUT invalid	0	-	ns
DS13	DSPI_SIN to DSPI_SCK input setup	3.2	-	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	-	ns
DS15	$\overline{DSPI\_SS}$ active to DSPI_SOUT driven	-	25	ns
DS16	$\overline{DSPI\_SS}$ inactive to DSPI_SOUT not driven	-	25	ns

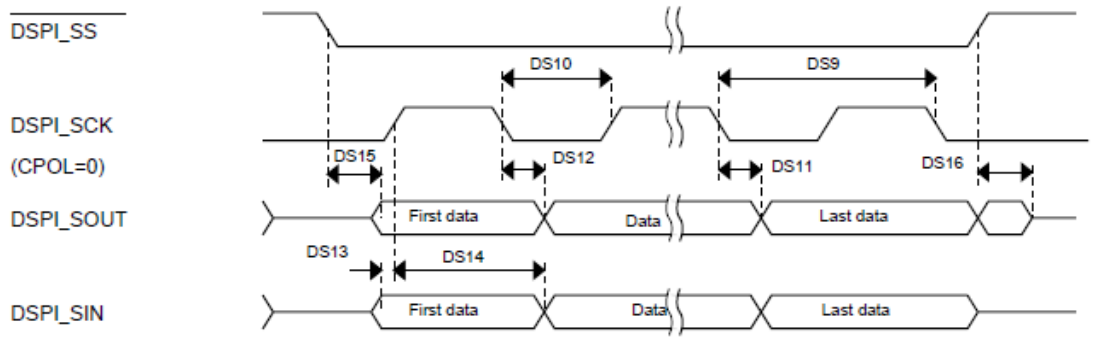


Figure 5: Slave mode DSPI timing.

4.6.4 Carrier Modulator Timer (CMT)

See also ⇨ 4.8 General Switching Specification.

Signal Name	Description	I/O	Pad
CMT_IRO	Carrier Modulator Transmitter Infrared Output	O	D2, E2

4.6.5 Touch Sensing Input (TSI)

Signal Name	Description	I/O	Signal	Pad
TSI0_CH[15:0]	Touch sensing input capacitive pins	I/O	TSI0_CH0	F5
			TSI0_CH1	F8
			TSI0_CH2	E6
			TSI0_CH3	F7
			TSI0_CH4	B5
			TSI0_CH5	B4
			TSI0_CH6	A8
			TSI0_CH7	B3
			TSI0_CH8	C4
			TSI0_CH9	C5

Signal Name	Description	I/O	Signal	Pad
			TSI0_CH10	B6
			TSI0_CH11	B2
			TSI0_CH12	C3
			TSI0_CH13	C2
			TSI0_CH14	E2
			TSI0_CH15	E1

TSI electrical specifications

Symbol	Description	Min.	Typ	Max.	Unit
T_a	Ambient temperature	-30	-	75	°C
TSI_RUNF	Fixed power consumption in run mode	-	100	-	µA
TSI_RUNV	Variable power consumption in run mode (depends on oscillator's current selection)	1	-	128	µA
TSI_EN	Power consumption in enable mode	-	100	-	µA
TSI_DIS	Power consumption in disable mode	-	1.2	-	µA
TSI_TEN	TSI analog enable time	-	66	-	µs
TSI_CREF	TSI reference capacitor	-	1	-	pF
TSI_DVOLT	Voltage variation of VP and VM around nominal values	0.19	-	1.03	V

4.6.6 General Purpose Input/Output (GPIO)

Signal Name	Description	I/O	GPIO	Pad
PTA[19:16][2:0]	General Purpose Input/Output	I/O	PTA0	C4
			PTA1	C5
			PTA2	A3
			PTA16	B6
			PTA17	B2
			PTA18	C3
			PTA19	C2
PTB[18][3:0]	General Purpose Input/Output	I/O	PTB0	D1
			PTB1	D2
			PTB2	D3
			PTB3	D4
			PTB18	F3
PTC[19:16][7:0]	General Purpose Input/Output	I/O	PTC0	E5
			PTC1	A8
			PTC2	E2

Signal Name	Description	I/O	GPIO	Pad
			PTC3	E1
			PTC4	F5
			PTC5	F8
			PTC6	E6
			PTC7	F7
			PTC16	B5
			PTC17	B4
			PTC18	A8
			PTC19	B3

The maximum input voltage on PTC0/1/2/3 is V_{DD}+0.3 V.

See also ⇨ 4.8 General Switching Specification.

4.6.7 Low-Leakage Wakeup (LLWU)

Signal Name	Description	I/O	Signal	Pad
LLWU_P[15:0]	Wakeup inputs	I	LLWU_P0	B5
			LLWU_P1	B4
			LLWU_P2	A8
			LLWU_P3	B3
			LLWU_P4	B6
			LLWU_P5	B2
			LLWU_P6	C3
			LLWU_P7	C2
			LLWU_P8	D1
			LLWU_P9	E5
			LLWU_P10	E2
			LLWU_P11	E1
			LLWU_P12	F5
			LLWU_P13	F8
			LLWU_P14	E6
			LLWU_P15	F7

4.6.8 Radio Module Signals

Signal Name	Description	I/O	Pad
DTM_RX	Direct test mode receive	I	B4, D2, E2
DTM_TX	Direct test mode transmit	O	A8, D3, E1
BSM_CLK	Bit streaming mode (BSM) clock signal, 802.15.4 packet data stream clock line	O	B3, F8
BSM_FRAME	Bit streaming mode frame signal, 802.15.4 packet data stream frame line	O	B4, E6
BSM_DATA	Bit streaming mode data signal, 802.15.4 packet data stream data line	I/O	A8, F5, F7
RF_RESET	Radio reset signal	I	B2
BLE_RF_ACTIVE	Signal to indicate future Bluetooth Low Energy activity.	O	B3, C6
RF_NOT_ALLOWED	Radio off signal, intended for Wi-Fi coexistence control	I	D3, F8
RX_SWITCH	Front end module receive mode signal	O	E1
TX_SWITCH	Front end module transmit mode signal	O	E2

4.6.9 Analog-to-Digital Converter (ADC)

Signal Name	Description	I/O	Signal	Pad
ADC0_DM0	ADC channel 0 differential input negative	I	ADC0_DM0	F4
ADC0_DP0	ADC channel 0 differential input positive	I	ADC0_DP0	F3
ADC0_SE[5:1]	ADC channel 0 single-ended input	I	ADC0_SE1	D2
			ADC0_SE2	D4
			ADC0_SE3	D3
			ADC0_SE4	F6
			ADC0_SE5	C2

16-bit ADC operating conditions

Symbol	Description	Min.	Typ[16]	Max.	Unit
V_{DDA}	Supply voltage absolute	1.71	-	3.6	V
V_{OUT}	Internally generated ADC reference voltage output	-	1.2	-	V
V_{REFL}	ADC reference voltage low	-	GND	-	

[16] Typical values assume V_{DDA}=3.0 V, Temp=25 °C, f_{ADCK}=1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.

Symbol	Description	Min.	Typ[16]	Max.	Unit
V_{ADIN}	Input voltage				
	16-bit differential mode	V_{REFL}	-	$31/32 \cdot V_{REFH}$	V
	All other modes	V_{REFL}	-	V_{REFH}	
C_{ADIN}	Input capacitance				
	16-bit mode	-	8	10	pF
	8-bit/10-bit/12-bit modes	-	4	5	
R_{ADIN}	Input series resistance	-	2	5	kΩ
R_{AS}	Analog source resistance (external) 13-bit/12-bit modes f_{ADCK}<4 MHz	-	-	5	kΩ
f_{ADCK}	ADC conversion clock frequency[17]				
	≤13-bit mode	1	-	18	MHz
	16-bit mode	2	-	12	
C_{rate}	ADC conversion rate				
	No ADC hardware averaging, continuous conversions enabled, subsequent conversion time				
	≤13-bit mode	20.000	-	818.330	ksps
	16-bit mode	37.037	-	461.467	

4.6.10 12-bit Digital-to-Analog Converter (DAC)

Signal Name	Description	I/O	Pad
DAC0_OUT	DAC output	O	F6

12-bit DAC operating requirements

Symbol	Description	Min.	Max.	Unit
V_{DDA}	Supply voltage	1.71	3.6	V
V_{DACR}	Reference voltage[18]	1.2	3.6	V
C_L	Output load capacitance[19]	-	100	pF
I_L	Output load current	-	1	mA

[17] To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.

[18] The DAC reference can be selected to be V_{DDA} or V_{REFH}=1.2 V.

[19] A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

12-bit DAC operating behaviors

Symbol	Description	Min.	Typ	Max.	Unit
I_{DDA_DACLP}	Supply current, low-power mode	-	-	250	µA
I_{DDA_DACHP}	Supply current, high speed mode	-	-	900	µA
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F), low-power mode[20]	-	100	200	µs
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F), high-speed mode[20]	-	15	30	µs
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08), low-power mode and high-speed mode[20]	-	0.7	1	µs
$V_{dacoutl}$	DAC output voltage range low - high-speed mode, no load, DAC set to 0x000	-	-	100	mV
$V_{dacouth}$	DAC output voltage range high – high-speed mode, no load, DAC set to 0xFFF	V_{DACR}-100	-	V_{DACR}	mV
INL	Integral non-linearity error, high-speed mode[21]	-	-	±8	LSB
DNL	Differential non-linearity error, V_{DACR} > 2 V[22]	-	-	±1	LSB
DNL	Differential non-linearity error, V_{DACR} =VREF_OUT[23]	-	-	±1	LSB
V_{OFFSET}	Offset error[24]	-	±0.4	±0.8	%FSR
E_G	Gain error[24]	-	±0.1	±0.6	%FSR
PSRR	Power supply rejection ratio, V_{DDA} ≥ 2.4 V	60	-	90	dB
T_{CO}	Temperature coefficient offset voltage[25]	-	3.7	-	µV/C
T_{GE}	Temperature coefficient gain error	-	0.000421	-	%FSR/C
R_{OP}	Output resistance (load=3 kΩ)	-	-	250	Ω

[20] Settling within ±1 LSB.

[21] The INL is measured for 0+100 mV to V_{DACR} -100 mV.

[22] The DNL is measured for 0+100 mV to V_{DACR} -100 mV.

[23] The DNL is measured for 0+100 mV to V_{DACR} -100 mV with V_{DDA}>2.4 V.

[24] Calculated by a best fit curve from V_{SS}+100 mV to V_{DACR} – 100 mV.

[25] V_{DDA}=3 V, reference select set for V_{DDA} (DACx_CO:DACRFS=1), high-power mode (DACx_C0:LPEN=0), DAC set to 0x800, temperature range is across the full range of the device.

Symbol	Description	Min.	Typ	Max.	Unit
SR	Slew rate				
	High-power	1.2	1.7		V/µs
	Low-power	0.05	0.12		
BW	3 dB bandwidth				
	High-power	550	-	-	kHz
	Low-power	40	-	-	

4.6.11 Analog Comparator (CMP)

Signal Name	Description	I/O	Signal	Pad
CMP0_IN[5:0]	Analog voltage inputs	I	CMP0_IN0	F3
			CMP0_IN1	F4
			CMP0_IN2	F6
			CMP0_IN3	D3
			CMP0_IN4	D4
			CMP0_IN5	D2
CMP0_OUT	Comparator output	O	CMP0_OUT	D1

CMP and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ	Max.	Unit
V_{DD}	Supply voltage	1.71	-	3.6	
I_{DDHS}	Supply current, high-speed mode (EN=1, PMODE=1)	-	-	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	-	-	20	µA
V_{AIN}	Analog input voltage	V_{SS}-0.3	-	V_{DD}	V
V_{AIO}	Analog input offset voltage	-	-	20	mV
V_H	Analog comparator hysteresis[26]				
	CR0[HYSTCTR]=00	-	5		mV
	CR0[HYSTCTR]=01	-	10	-	
	CR0[HYSTCTR]=10	-	20	-	
	CR0[HYSTCTR]=11	-	30	-	
V_{CMPOh}	Output high	V_{DD}-0.5	-	-	V
V_{CMPOl}	Output low	-	-	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns

[26] Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}-0.6 V.

Symbol	Description	Min.	Typ	Max.	Unit
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[27]	-	-	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	-	7	-	µA
INL	6-bit DAC integral non-linearity	-0.5	-	0.5	LSB[28]
DNL	6-bit DAC differential non-linearity	-0.3	-	0.3	LSB

4.6.12 Timer

Signal Name	Module	Description	I/O	Signal	Pad
TPM_CLKIN[1:0]	TPM0	External clock	I	TPM_CLKIN0	F6
				TPM_CLKIN1	B2
TPM0_CH[3:0]	TPM0	TPM channel	I/O	TPM0_CH0	F6,B2
				TPM0_CH1	D1, E1
				TPM0_CH2	C6, D2
				TPM0_CH3	A3, B5
TPM_CLKIN[1:0]	TPM1	External clock	I	TPM_CLKIN0	F6
				TPM_CLKIN1	B2
TPM1_CH[1:0]	TPM1	TPM channel	I/O	TPM1_CH0	C4, C5, F5
				TPM1_CH1	D3, D4, F8
TPM_CLKIN[1:0]	TPM2	External clock	I	TPM_CLKIN0	F6
				TPM_CLKIN1	B2
TPM2_CH[1:0]	TPM2	TPM channel	I/O	TPM2_CH0	C3, E6
				TPM2_CH1	C2, F7
LPTMR0_ALT[2:1]	LPTMR0	Pulse counter input pin	I	LPTMR0_ALT1	D2
				LPTMR0_ALT2	F8
RTC_CLKOUT	RTC Module	1 Hz square-wave output	O	RTC_CLKOUT	D4

4.6.13 Clocks

Signal Name	Description	I/O	Pad
CLKOUT	Internal clocks monitor	O	D1, D4
XTAL_OUT_EN	32 MHz clock output enable	I	D1, E6

[27] Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.

[28] 1 LSB=$V_{reference}$/64

4.6.14 Serial Wire Debug (SWD)

Signal Name	Description	Comment	I/O	Pad
SWD_DIO	Serial wire debug data Input/Output	Pulled up internally by default	I/O	C4
SWD_CLK	Serial wire clock	Pulled down internally by default	I	C5

SWD full voltage range electricals

See ⇨ Figure 6 and ⇨ Figure 7.

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation	-	25	MHz
J2	SWD_CLK cycle period	1/J1	-	ns
J3	SWD_CLK clock pulse width	20	-	ns
J4	SWD_CLK rise and fall times	-	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	-	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	-	ns
J11	SWD_CLK high to SWD_DIO data valid	-	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	-	ns

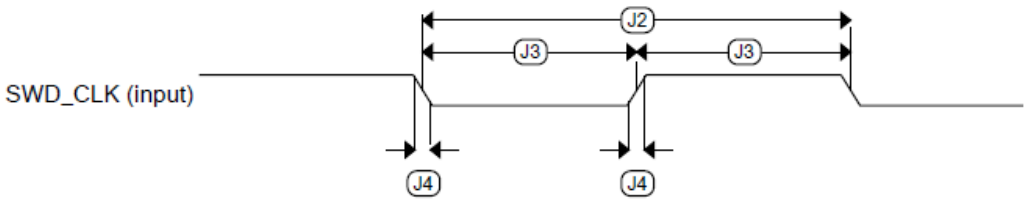


Figure 6: SWD clock input timing.

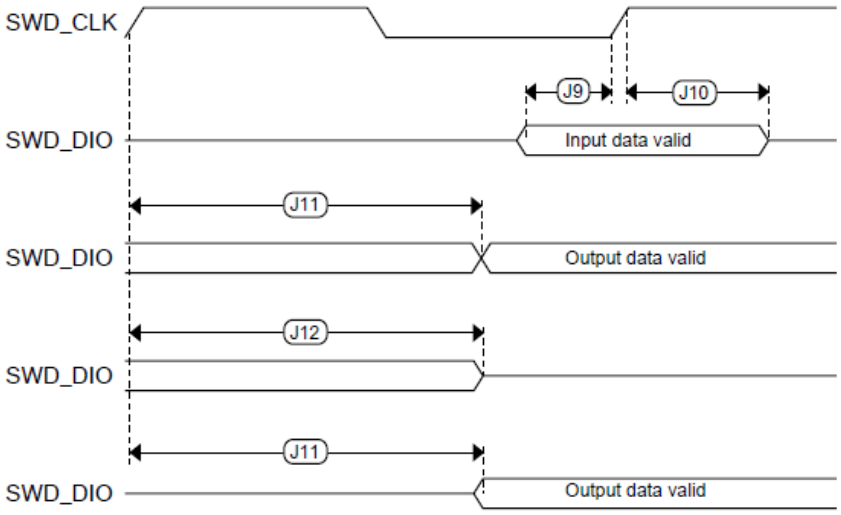


Figure 7: SWD data timing.

4.7 Flash Electrical Specifications

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Flash timing specifications (program and erase)

Symbol	Description	Min.	Typ	Max.	Unit
t_{hvpgm4}	Longword program high-voltage time	-	7.5	18	µs
$t_{hversscr}$	Sector erase high-voltage time[29]	-	13	113	ms
$t_{hversblk256k}$	Erase block high-voltage time for 256 KB[29]	-	104	904	ms

Flash timing specifications (commands)

Symbol	Description	Min.	Typ	Max.	Unit
$t_{rd1blk256k}$	Read 1s block execution time[30] 256 KB program flash	-	-	1.7	ms
$t_{rd1sec2k}$	Read 1s section execution time (flash sector)[30]	-	-	60	µs
t_{pgmchk}	Program check execution time[30]	-	-	45	µs
t_{rdrsrc}	Read resource execution time[30]	-	-	30	µs
t_{pgm4}	Program longword execution time	-	65	145	µs

[29]Maximum time based on expectations at cycling end-of-life.

[30]Assumes 25 MHz flash clock frequency.

Symbol	Description	Min.	Typ	Max.	Unit
$t_{ersblk256k}$	Erase flash block execution time[31] 256 KB program flash	-	250	1 500	ms
t_{ersscr}	Erase flash sector execution time[31]	-	14	114	ms
t_{rd1all}	Read 1s all blocks execution time[30]	-	-	1.8	ms
t_{rdonce}	Read once execution time[30]	-	-	30	µs
$t_{pgmonce}$	Program once execution time	-	100	-	µs
t_{ersall}	Erase all blocks execution time[31]	-	500	3 000	ms
t_{vfykey}	Verify backdoor access key execution time[30]	-	-	30	µs
$t_{ersallu}$	Erase all blocks unsecure execution time[31]	-	500	3 000	ms

Flash high voltage current behaviors

Symbol	Description	Min.	Typ	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	-	2.5	6	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	-	1.5	4	mA

4.8 General Switching Specification

These specifications apply to GPIO, LPUART, CMT, and I2C signals.

Description	Min.	Max.	Unit
GPIO pin interrupt pulse width (digital glitch filter disabled), Synchronous path[32],[33]	1.5	-	Bus clock cycles
Reset pin interrupt pulse width (analog filter enabled), Asynchronous path[34]	200	-	ns
GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled), Asynchronous path[5]	20	-	ns
External RESET_b input pulse width (digital glitch filter disabled)	100	-	ns

[31]Maximum times for erase parameters based on expectations at cycling end-of-life.

[32]This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry in run modes.

[33]The greater of synchronous and asynchronous timing must be met.

[34]This is the minimum pulse width that is guaranteed to be recognized.

Description		Min.	Max.	Unit
Port rise and fall time (low drive strength)[35,36]				
Slew enabled	1.71 ≤ V_{DD} ≤ 2.7 V	-	25	ns
	2.7 ≤ V_{DD} ≤ 3.6 V	-	16	
Slew disabled	1.71 ≤ V_{DD} ≤ 2.7 V	-	8	
	2.7 ≤ V_{DD} ≤ 3.6 V	-	6	
Port rise and fall time (low drive strength)[37,38]				
Slew enabled	1.71 ≤ V_{DD} ≤ 2.7 V	-	24	ns
	2.7 ≤ V_{DD} ≤ 3.6 V	-	16	
Slew disabled	1.71 ≤ V_{DD} ≤ 2.7 V	-	10	
	2.7 ≤ V_{DD} ≤ 3.6 V	-	6	

[35] PTB0, PTB1, PTC0, PTC1, PTC2, PTC3, PTC6, PTC7, PTC17, PTC18.

[36] 75 pF load.

[37] Ports A, B, and C

[38] 25 pF load

4.9 Transceiver Feature Summary

The PAN4620 module meets or exceeds all Bluetooth Low Energy 4.2 and IEEE 802.15.4 performance specifications applicable to 2.4 GHz ISM and MBAN (Medical Band Area Network) bands.

4.9.1 Channel Plan

Channel Plan for Bluetooth Low Energy

Band	Carrier frequency [MHz][39]	Channel number k
ISM	2 402+k·2	k=[0,1,…,38,39]

Channel Plan for IEEE 802.15.4

Band	Carrier frequency [MHz][40]	Channel number k
ISM	2 405+(k-11)·5	k=[11,12,…,25,26]
MBAN	2 363+k·5	k=[0,1,2,3,4,5,6]
	2 367+(k-7)·5	k=[7,8,9,10,11,12,14]

4.9.2 Receiver Feature Summary

The current consumption and sensitivity depend on the user scenario.

Assume V_{DD}=3.6 V, T_{amb}=25 °C, if nothing else is stated.

Symbol	Description[40]	Min.	Typ.	Max.	Unit
I_{RXon}	Supply current RX On (V_{DD}=3.6 V)[41]	-	6.8	-	mA
f_{IN}	Input RF frequency	2.36	-	2.4835	GHz
$SENS_{GFSK}$	GFSK RX sensitivity (250 kbps GFSK-BT=0.5, h=0.5)	-	-100	-	dBm
$SENS_{BLE}$	Bluetooth Low Energy RX sensitivity[42]	-	-95	-	dBm
$SENS_{15.4}$	IEEE 802.15.4 RX sensitivity[43]	-	-100	-	dBm
$RSSI_{Range}$	Receiver signal strength indicator range[44]	-100	-	5	dBm

[39] All the RX parameters are measured at the PAN4620 RF bottom pad.

[40] All the RX parameters are measured at the PAN4620 RF bottom pad.

[41] Transceiver power consumption. (As opposed to overall module power consumption.)

[42] Measured at 0.1 % BER using 37 byte long packets in max. gain mode and nominal conditions.

[43] In max. gain mode and nominal conditions.

[44] RSSI performance in narrowband mode.

Symbol	Description[40]	Min.	Typ.	Max.	Unit
$RSSI_{Res}$	Receiver signal strength indicator resolution	-	1	-	dBm
	Typical RSSI variation over frequency	-2	-	2	dB
	Typical RSSI variation over temperature	2	-	2	dB
$RSSI_{ACC}$	Narrowband RSSI accuracy[45]	-3	-	3	dBm
$BLE_{co\text{-}channel}$	Bluetooth Low Energy Co-channel Interference (Wanted signal at -67 dBm, BER <0.1 %. Measurement resolution 1 MHz)	-	-7	-	dB
$15.4_{co\text{-}channel}$	IEEE 802.15.4 Co-channel Interference (Wanted signal 3 dB over reference sensitivity level)	-	-2	-	dB

4.9.3 Transmitter Feature Summary

The current consumption and output power depend on the user scenario.

Assume V_{DD}=3.6 V, T_{amb}=25 °C, if nothing else is stated.

Symbol	Description[46]	Min.	Typ.	Max.	Unit
I_{TXon}[47]	Supply current TX On with P_{RF}=0 dBm (V_{DD}=3.6 V)	-	6.1	-	mA
f_c	Output Frequency	2.36	-	2.4835	GHz
P_{RFmax}	Maximum RF Output power	-	3.5	-	dBm
P_{RFmin}	Minimum RF Output power	-	-30	-	dBm
P_{RFCR}	RF Output power control range	-	33.5	-	dB
$F_{dev15.4}$	IEEE 802.15.4 Peak frequency deviation	-	500	-	kHz
$EVM_{15.4}$	IEEE 802.15.4 Error Vector Magnitude (EVM)[48]	-	4.5	-	%
$\Delta f1_{avg,BLE}$	Bluetooth Low Energy average frequency deviation using a 00001111 modulation sequence	-	250	-	kHz
$\Delta f2_{avg,BLE}$	Bluetooth Low Energy average frequency deviation using a 01010101 modulation sequence	-	220	-	kHz
$F_{cdev,BLE}$[49]	Bluetooth Low Energy Maximum Deviation of the Center Frequency	-	10	-	kHz

[45] With one point calibration over frequency and temperature.

[46] All the TX parameters are measured at the chip RF output.

[47] Receiver power consumption. (As opposed to overall module power consumption.)

[48] Measured as per IEEE Standard 802.15.4

[49] Maximum drift of carrier frequency of the PLL during a BLE packet with a nominal 32 MHz reference crystal.

Symbol	Description[46]	Min.	Typ.	Max.	Unit
	Bluetooth Low Energy Frequency Hopping Support		Yes		
TXH2	2nd Harmonic of Transmit Carrier Frequency (for $P_{out}=P_{RF,max}$),	-	-65	-	dBm/ MHz
TXH3	3rd Harmonic of Transmit Carrier Frequency (for $P_{out}=P_{RF,max}$),	-	-41	-	dBm/ MHz

Transmitter output power temperature dependence

Symbol	Description[50]	-40 °C	25 °C	75 °C	Unit
$P_{RF,max}$	Typical maximum RF Output power	4.5	3.5	2.1	dBm
$P_{RF,min}$	Typical minimum RF Output power	-30.1	-31.1	-32.6	dBm

4.10 Reliability Tests

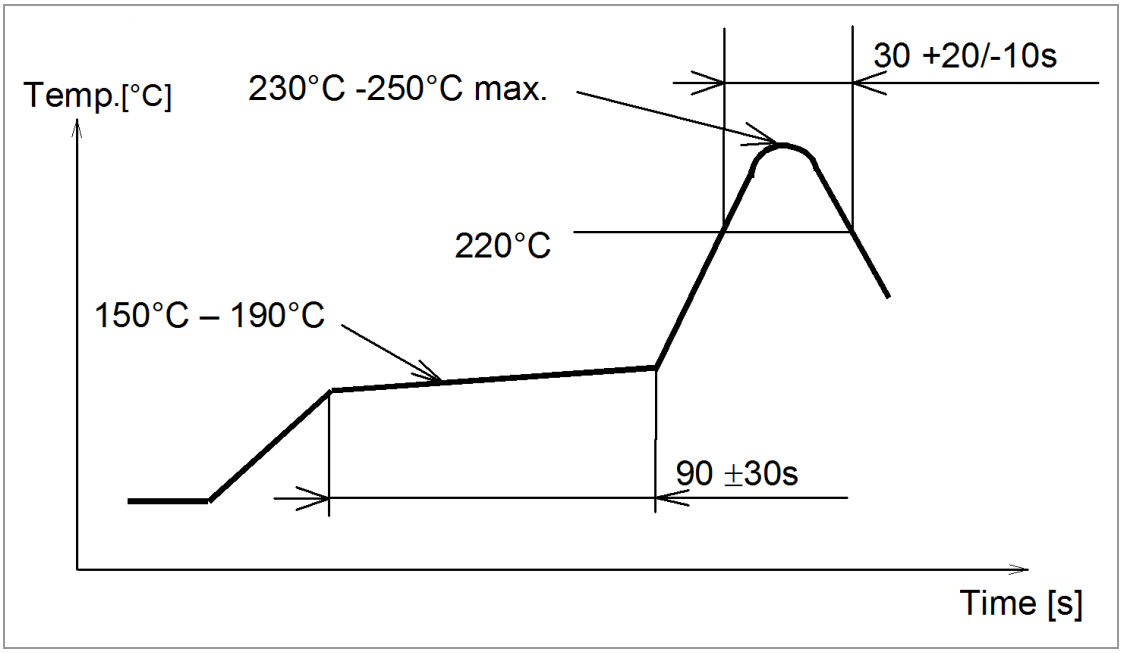
The measurement should be done after the test device has been exposed to room temperature and humidity for one hour.

No.	Item	Limit	Condition
1	Variable Vibration Test (VVT)	Electrical parameter should be in specification	Freq.: 20~2 000 Hz, Acc.: 17 50 G, Sweep: 8 min, 2 hours each of XYZ axis
2	Shock Drop Test (DT)	Electrical parameter should be in specification	Drop parts on concrete from a height of 1 m for 3 times
3	Heat-Shock/ Temperature Cycling Test (TC)	Electrical parameter should be in specification	at -40 °C and +75 °C for 1 h/cycle Total=300 cycles
4	Temperature Humidity Bias Test (THB)	Electrical parameter should be in specification	At +60 °C, 85 % r.H., 300 h
5	Low Temperature Storage Life Test (LTSL)	Electrical parameter should be in specification	At -40 °C, 300 h
6	High Temperature Storage Life Test (HTSL)	Electrical parameter should be in specification	At +85 °C, 300 h

[50] All the TX parameters are measured at the chip RF output.

4.11 Recommended Soldering Profile

- Reflow permissible cycles: 2
- Opposite side reflow is prohibited due to module weight
- More than 75 percent of the soldering area shall be coated by solder
- The soldering profiles should be adhered to in order to prevent electrical or mechanical damage
- Soldering profile assumes lead-free soldering



5 Cautions

Failure to follow the guidelines set forth in this document may result in degrading of the module functions and damage to the module.

5.1 Design Notes

1. Follow the conditions written in this specification, especially the control signals of this module.
2. The supply voltage should abide by the maximum ratings (⇨ 4.2 Absolute Maximum Ratings).
3. The supply voltage must be free of AC ripple voltage (for example from a battery or a low noise regulator output). For noisy supply voltages, provide a decoupling circuit (for example a ferrite in series connection and a bypass capacitor to ground of at least 47 µF directly at the module).
4. This module should not be mechanically stressed when installed.
5. Keep this module away from heat. Heat is the major cause of decreasing the life time of these modules.
6. Avoid assembly and use of the target equipment in conditions where the module temperature may exceed the maximum tolerance.
7. Keep this module away from other high frequency circuits.
8. Refer to the recommended pattern when designing a board.

5.2 Installation Notes

1. Reflow soldering is possible twice based on the conditions set forth in ⇨ 4.11 Recommended Soldering Profile. Set up the temperature at the soldering portion of this module according to this reflow profile.
2. Carefully position the module so that the heat will not burn into printed circuit boards or affect other components that are susceptible to heat.
3. Carefully locate the module, to avoid an increased temperature caused by heat generated by neighboring components.
4. If a vinyl-covered wire comes into contact with the module, the wire cover will melt and generate toxic gas, damaging the insulation. Never allow contact between a vinyl cover and these modules to occur.
5. This module should not be mechanically stressed or vibrated when reflowed.
6. To repair the board by hand soldering, follow the conditions set forth in this chapter.
7. Do not wash this product.
8. Pressing on parts of the metal cover or fastening objects to the metal will cause damage to the module.

5.3 Usage Condition Notes

1. Take measures to protect the module against static electricity.
   If pulses or transient loads (a large load, which is suddenly applied) are applied to the modules, check and evaluate their operation before assembly of the final products.
2. Do not use dropped modules.
3. Do not touch, damage, or soil the pins.
4. Follow the recommended condition ratings about the power supply applied to this module.
5. Electrode peeling strength: Do not apply a force of more than 4.9 N in any direction on the soldered module.
6. Pressing on parts of the metal cover or fastening objects to the metal cover will cause damage.
7. These modules are intended for general purpose and standard use in general electronic equipment, such as home appliances, office equipment, information, and communication equipment.

5.4 Storage Notes

1. The module should not be stressed mechanically during storage.
2. Do not store these modules in the following conditions or the performance characteristics of the module, such as RF performance will be adversely affected:

– Storage in salty air or in an environment with a high concentration of corrosive gas, such as Cl_2, H_2S, NH_3, SO_2, or NO_X,
– Storage in direct sunlight,
– Storage in an environment where the temperature may be outside the range of 5 °C to 35 °C, or where the humidity may be outside the 45 % to 85 % range,
– Storage of the modules for more than one year after the date of delivery storage period: Please check the adhesive strength of the embossed tape and soldering after 6 months of storage.

3. Keep this module away from water, poisonous gas, and corrosive gas.
4. This module should not be stressed or shocked when transported.
5. Follow the specification when stacking packed crates (max. 10).

5.5 Safety Cautions

These specifications are intended to preserve the quality assurance of products and individual components.

Before use, check and evaluate the operation when mounted on your products. Abide by these specifications without deviation when using the products. These products may short-circuit. If electrical shocks, smoke, fire, and/or accidents involving human life are anticipated when a short circuit occurs, provide the following failsafe functions as a minimum:

1. Ensure the safety of the whole system by installing a protection circuit and a protection device.
2. Ensure the safety of the whole system by installing a redundant circuit or another system to prevent a single fault causing an unsafe status.

5.6 Other Cautions

1. Do not use the module for other purposes than those listed in ⇨ 5.3 Usage Condition Notes.
2. Be sure to provide an appropriate fail-safe function on your product to prevent any additional damage that may be caused by the abnormal function or the failure of the module.
3. This module has been manufactured without any ozone chemical controlled under the Montreal Protocol.
4. These modules are not intended for use under the special conditions shown below. Before using these modules under such special conditions, carefully check their performance and reliability under the said special conditions to determine whether or not they can be used in such a manner:

– In liquid, such as water, salt water, oil, alkali, or organic solvent, or in places where liquid may splash,
– In direct sunlight, outdoors, or in a dusty environment,
– In an environment where condensation occurs,
– In an environment with a high concentration of harmful gas (e. g. salty air, HCl, Cl_2, SO_2, H_2S, NH_3, and NO_X).

5. If an abnormal voltage is applied due to a problem occurring in other components or circuits, replace these modules with new modules, because they may not be able to provide normal performance even if their electronic characteristics and appearances appear satisfactory.
6. When you have any question or uncertainty, contact Panasonic.

5.7 Restricted Use

5.7.1 Life Support Policy

This Panasonic Industrial Devices Europe GmbH product is not designed for use in life support appliances, devices, or systems where malfunction can reasonably be expected to result in a significant personal injury to the user, or as a critical component in any life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Panasonic customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Panasonic Industrial Devices Europe GmbH for any damages resulting.

5.7.2 Restricted End Use

This Panasonic Industrial Devices Europe GmbH product is not designed for any restricted activity that supports the development, production, handling usage, maintenance, storage, inventory or proliferation of any weapons or military use.

Transfer, export, re-export, usage or reselling of this product to any destination, end user or any end use prohibited by the European Union, United States or any other applicable law is strictly prohibited.

6 Regulatory and Certification Information

The RF synthesizer within the PAN4620 can be configured to use any channel frequency between 2.36 GHz and 2.487 GHz. However, the information given in ⇨ 6 Regulatory and Certification Information is only valid within the ISM frequency band starting at 2.4 GHz. To not void the precertification and to be sure you are not violating regulatory requirements, use the certified Bluetooth LE, Thread, and Zigbee wireless stacks.

To not void the precertification and to ensure compliance with regulatory requirements study the integration guide for this module carefully and follow the given instructions.

The Integration guide can be downloaded ⇨ 1.4 Related Documents.

6.1 Federal Communications Commission (FCC) for US

6.1.1 FCC Notice

The PAN4620 including the antennas, which are listed in ⇨ 6.1.5 Approved Antenna List, complies with Part 15 of the FCC Rules.

The device meets the requirements for modular transmitter approval as detailed in FCC public Notice DA00-1407. The transmitter operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation.

6.1.2 Caution

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by Panasonic Industrial Devices Europe GmbH may void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules.

These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.

However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna,
- Increase the separation between the equipment and receiver,
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected,
- Consult the dealer or an experienced radio/TV technician for help.

6.1.3 Label Requirements

The OEM must ensure that FCC labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Panasonic FCC identifier for this product as well as the FCC Notice above.

The FCC identifier is **FCC ID: T7V4620**.

This FCC identifier is valid for the PAN4620. The end product must in any case be labelled on the exterior with:

"Contains FCC ID: T7V4620"

6.1.4 Antenna Warning

This antenna warning refers to the test device with the model number PAN4620
⇨ 7.1 Ordering Information

The device is tested with a standard SMA connector and with the antenna listed below. When integrated into the OEM's product, these fixed antennas require installation preventing end users from replacing them with non-approved antennas. Any antenna not in the following table must be tested to comply with FCC Section 15.203 for unique antenna connectors and with Section 15.247 for emissions. The FCC identifier for the device with the antenna listed in ⇨ 6.1.5 Approved Antenna List is the same (**FCC ID: T7V4620**).

6.1.5 Approved Antenna List

Item	Part Number	Manufacturer	Frequency Band	Type	Max. Gain (dBi)
1	ANT016008LCS2442MA1	TDK	2.4 GHz	Chip antenna	1.6

6.1.6 RF Exposure

To comply with FCC RF Exposure requirements, the OEM must ensure that only antennas from the Approved Antenna List are installed ⇨ 6.1.5 Approved Antenna List.

The preceding statement must be included as a CAUTION statement in manuals for products operating with the approved antennas in the previous table to alert users on FCC RF Exposure compliance.

Any notification to the end user of installation or removal instructions about the integrated radio module is not allowed.

The radiated output power of the PAN4620 with a mounted ceramic antenna (**FCC ID: T7V4620**) is below the FCC radio frequency exposure limits. Nevertheless, the PAN4620 shall be used in such a manner that the potential for human contact during normal operation is minimized.

End users may not be provided with the module installation instructions. OEM integrators and end users must be provided with transmitter operating conditions for satisfying RF exposure compliance.

6.1.7 Integration Instructions for Host Product Manufacturers According to KDB 996369 D03 OEM Manual v01

Section	Topic and comment
2.2	**List of applicable FCC rules** FCC part 15.247 operation within the bands 902 MHz to 928 MHz, 2 400 MHz to 2 483.5 MHZ, and 5 725 MHz to 5 850 MHz.
2.3	**Specific operational use conditions** Please refer to ⇨ 5 Cautions and especially part ⇨ 5.3 Usage Condition Notes.
2.4	**Limited module procedures** Not applicable This has a single-modular transmitter approval.
2.5	**Trace antenna designs** Not applicable The module has a ceramic chip antenna instead of a trace antenna. For guidance regarding the PCB layout please refer to the PAN4620 Integration Guide ⇨ 7.3.2 Product Information.

Section	Topic and comment
2.6	**RF exposure considerations** Please refer to ⇨ 6.1.6 RF Exposure and also read the “PAN4620 Integration Guide” carefully ⇨ 7.3.2 Product Information. The FCC test report for the PAN4620 states that the power density levels for FCC at a distance of 20 cm are below the maximum levels allowed by regulations.
2.7	**Antennas** For information about the antenna configuration please refer to ⇨ 6.1.4 Antenna Warning and ⇨ 6.1.5 Approved Antenna List.
2.8	**Label and compliance information** For guidance regarding the required labeling please refer to ⇨ 6.1.3 Label Requirements.
2.9	**Information on test modes and additional testing requirements** Please read the “PAN4620 Integration Guide” carefully ⇨ 7.3.2 Product Information. It offers guidance for PCB Layout and also relevant software.
2.10	**Additional testing, Part 15 Subpart B disclaimer** The PAN4620 is only FCC authorized for the specific rule FCC part 15.247. The host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the PAN4620 installed.

6.2 Innovation, Science, and Economic Development (ISED) for Canada

English

The PAN4620 is licensed to meet the regulatory requirements of ISED.

License ID: **IC: 216Q-4620**

Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and ensure compliance for SAR and/or RF exposure limits. Users can obtain Canadian information on RF exposure and compliance from www.ic.gc.ca.

This device has been designed to operate with the antennas listed in ⇨ 6.1.5 Approved Antenna List, having a maximum gain of +1.6 dBi. Antennas not included in this list or having a gain greater than +1.6 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms. The antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Due to the model size, the IC identifier is displayed in the installation instruction only and it cannot be displayed on the module’s label due to the limited size.

French

PAN1762 est garanti conforme aux dispositions règlementaires d’Industry Canada (ISED).

License: **IC: 216Q-4620**

Il est recommandé aux fabricants d'appareils fixes, mobiles ou portables de consulter la réglementation en vigueur et de vérifier la conformité de leurs produits relativement aux limites d'exposition aux rayonnements radiofréquence ainsi qu'au débit d'absorption spécifique maximum autorisé.

Des informations pour les utilisateurs sur la réglementation Canadienne concernant l'exposition aux rayonnements RF sont disponibles sur le site www.ic.gc.ca.

Ce produit a été développé pour fonctionner spécifiquement avec les antennes listées dans le tableau ⇨ 6.1.5 Approved Antenna List, présentant un gain maximum de 1.6 dBi. Des antennes autres que celles listées ici, ou présentant un gain supérieur à 1.6 dBi ne doivent en aucune circonstance être utilisées en combinaison avec ce produit. L'impédance des antennes compatibles est 50 Ohm. L'antenne utilisée avec ce produit ne doit ni être située à proximité d'une autre antenne ou d'un autre émetteur, ni être utilisée conjointement avec une autre antenne ou un autre émetteur.

En raison de la taille du produit, l'identifiant IC est fourni dans le manuel d'installation.

6.2.1 IC Notice

English

The device PAN4620 (⇨ 7.1 Ordering Information), including the antennas (⇨ 6.1.5 Approved Antenna List), complies with Canada RSS-GEN Rules. The device meets the requirements for modular transmitter approval as detailed in RSS-Gen.

Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation.

French

Le présent appareil PAN4620 (⇨ 7.1 Ordering Information), les antennes y compris (⇨ 6.1.5 Approved Antenna List), est conforme aux CNR-Gen d'Industrie Canada applicables aux appareils radio exempts de licence.

L'exploitation est autorisée aux deux conditions suivantes:

1. L'appareil ne doit pas produire de brouillage, et
2. L'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

6.2.2 Labeling Requirements

English

Labeling Requirements

The OEM must ensure that IC labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Panasonic IC identifier for this product as well as the IC Notice above.

The IC identifier is:

IC: 216Q-4620

This IC identifier is valid for all PAN4620 modules ⇨ 7.1 Ordering Information. In any case, the end product must be labelled on the exterior with:

"Contains IC: 216Q-4620”.

French

Obligations d’étiquetage

Les fabricants d’équipements d’origine (FEO) – en anglais Original Equipment Manufacturer (OEM) – doivent s’assurer que les obligations d’étiquetage IC du produit final sont remplies. Ces obligations incluent une étiquette clairement visible à l’extérieur de l’emballage externe, comportant l’identifiant IC du module Panasonic inclus, ainsi que la notification ci-dessus.

L’ identifiant IC est:

IC: 216Q-4620

Cet identifiant est valide pour tous les modules PAN4620 ⇨ 7.1 Ordering Information. Dans tous les cas les produits finaux doivent indiquer sur leur emballage externe la mention suivante:

"Contient IC: 216Q-4620”.

6.3 European Conformity According to RED (2014/53/EU)

All modules described in this Product Specification comply with the standards according to the following LVD (2014/35/EU), EMC-D (2014/30/EU) together with RED (2014/53/EU) articles:

3.1a Safety/Health:	EN 62368-1:2014
	EN 62311:2008

3.1b EMC:	EN 301 489-1 V2.1.1:2017-02
	EN 301 489-17 V3.1.1:2017-02
3.2 Radio:	EN 300 328 V2.1.1:2016-11

As a result of the conformity assessment procedure described in 2014/53/EU Directive, the end customer equipment should be labelled as follows:

CE

The end customer has to assure that the device has a distance of more than 20 cm from the human body under all circumstances.

The end customer equipment must meet the actual Safety/Health requirements according to RED.

PAN4620 and its model versions in the specified reference design can be used in all countries of the European Economic Area (Member States of the EU, European Free Trade Association States [Iceland, Liechtenstein, Norway]), Monaco, San Marino, Andorra, and Turkey.

6.4 Bluetooth

Bluetooth end products which integrate the PAN4620 need to receive the following IDs at creation:

Bluetooth 4.2	Declaration ID	QDID
Component (Tested)	D031669	84040
Component (Tested)	D031668	84041
End Product	D044186	131815

Bluetooth Marks

According to the Bluetooth SIG, the PAN4620 fulfills the criteria to label your product as a Bluetooth device:

For further information please refer to the Bluetooth website www.bluetooth.com.

6.5 RoHS and REACH Declaration

The latest declaration of environmental compatibility (Restriction of Hazardous Substances, RoHS and Registration, Evaluation, Authorisation and Restriction of Chemicals, REACH) for supplied products can be found on the Panasonic website in the “Downloads” section of the respective product ⇨ 7.3.2 Product Information.

7 Appendix

7.1 Ordering Information

Variants and Versions

Order Number	Brand Name	Description	MOQ[51]
ENWC9B01A1EF	PAN4620	IEEE 802.15.4 and Bluetooth Low Energy Module	500

[51]The default MOQ for mass production is 500 pieces, fewer only on customer demand. Samples for evaluation can be delivered at any quantity via the distribution channels.

7.2 List of Acronyms

ADC ..... *Analog-to-digital converter*
CMP ..... *Analog comparator*
DAC ..... *Digital-to-analog converter*
DSPI ..... *DMA Serial peripheral interface*
DT ..... *Shock drop test*
EUI ..... *Extended Unique Identifier*
EVM ..... *Error vector magnitude*
GPIO ..... *General purpose Input/Output*
HTSL ..... *High temperature storage life test*
I^2C ..... *Inter-integrated circuit*
LLWU ..... *Low-leakage wakeup*
LTSL ..... *Low temperature storage life test*
MBAN ..... *Medical band area network*
MOQ ..... *Minimum order quantity*
OUI ..... *Organizationally Unique Identifier*
SPI ..... *Serial peripheral interface*
SWD ..... *Serial wire debug*
TC ..... *Heat-shock/ temperature cycling test*
THB ..... *Temperature humidity bias test*
TPM ..... *Timers module*
TSI ..... *Touch sensing input*
VVT ..... *Variable vibration test*

7.3 Contact Details

7.3.1 Contact Us

Please contact your local Panasonic Sales office for details on additional product options and services:

For Panasonic Sales assistance in the **EU**, visit
https://eu.industrial.panasonic.com/about-us/contact-us
Email: wireless@eu.panasonic.com

For Panasonic Sales assistance in **North America**, visit the Panasonic website "Sales & Support" to find assistance near you at
https://na.industrial.panasonic.com/distributors

Please visit the **Panasonic Wireless Technical Forum** to submit a question at
https://forum.na.industrial.panasonic.com

7.3.2 Product Information

Please refer to the Panasonic Wireless Connectivity website for further information on our products and related documents:

For complete Panasonic product details in the **EU**, visit
http://pideu.panasonic.de/products/wireless-modules.html

For complete Panasonic product details in **North America**, visit
http://www.panasonic.com/rfmodules